

Round Rock 13.3" Schematics Document

Haswell ULT

2013-06-28
REV : SSI

DY : None Installed
XDP: For CPU XDP Debug Port installed
PCH_XDP: For PCH XDP Debug Port installed

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Round Rock 13.3" UMA

Rev
X00

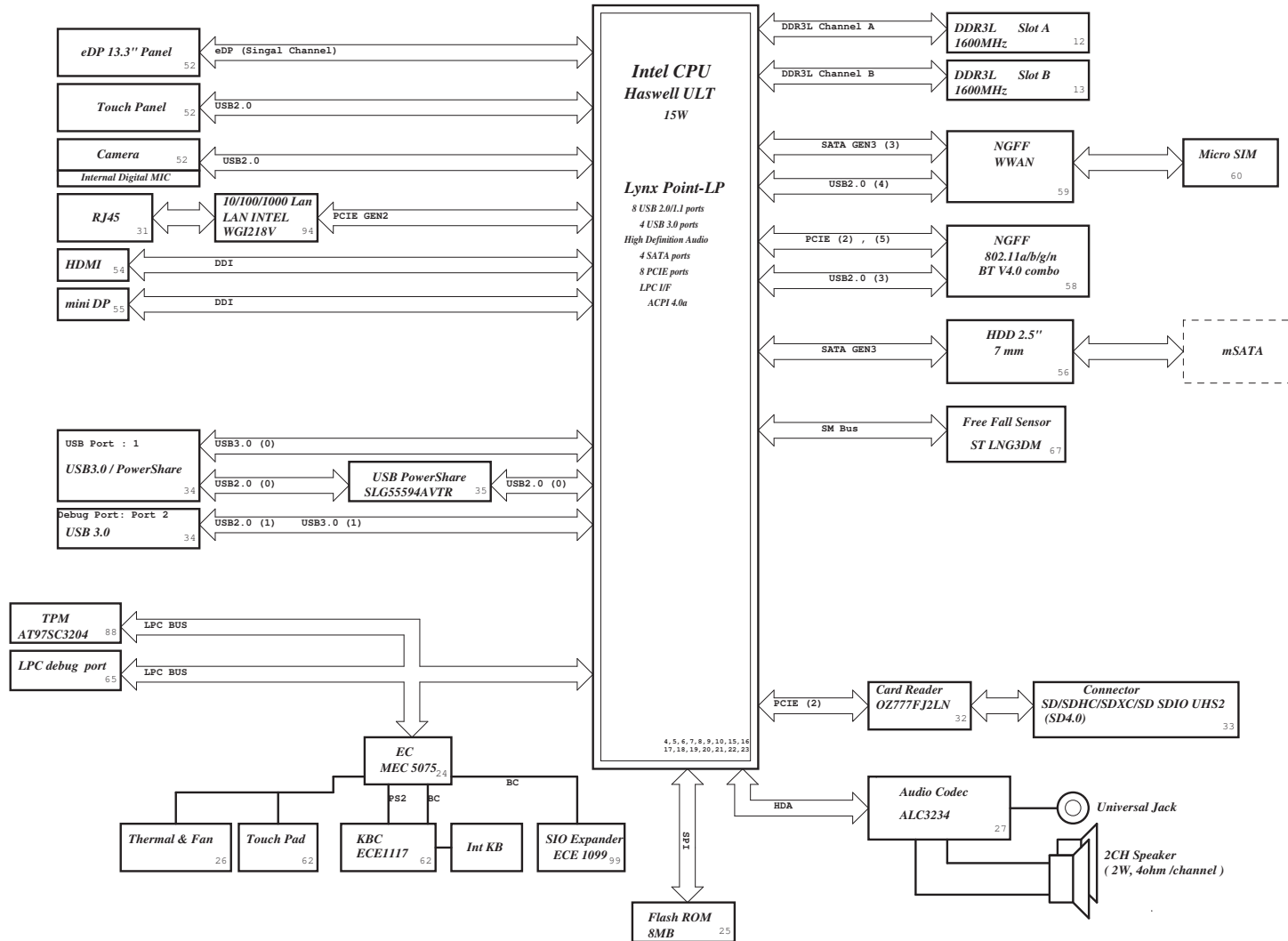
Date: Friday, June 28, 2013

Sheet 1 of 107

Round Rock 13.3" Block Diagram

Project code : 91.40A01.001
PCB P/N : 13229
Revision : X00

CHARGER BQ24715 44	
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC TPS51275 45	
INPUTS	OUTPUTS
DCRATOUT	3.3V_AUX_S5 3.3V_S5 5V_S5
CPU DC/DC TPS51622 46~47	
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE
SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCRATOUT	ID05V_M
SYSTEM DC/DC TPS51363 & APL5338 49	
INPUTS	OUTPUTS
DCRATOUT	ID05V_S3 ID0675V_S0 DDR_VREF_S3
Load Switches 36	
INPUTS	OUTPUTS
5V_S3 3.3V_S3	5V_S0 3.3V_S0 3.3V_SS_PCH 3.3V_M 3.3V_LAN ID05V_MODPHY ID05V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top L2:Power/GND L3:Signal L4:Signal L5:Power/GND	L6:Bottom



<Core Design>

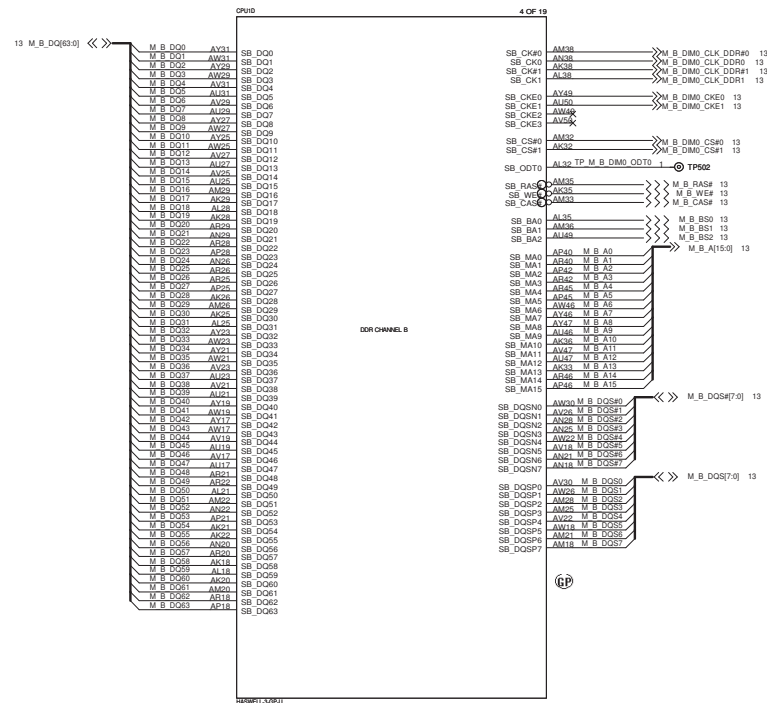
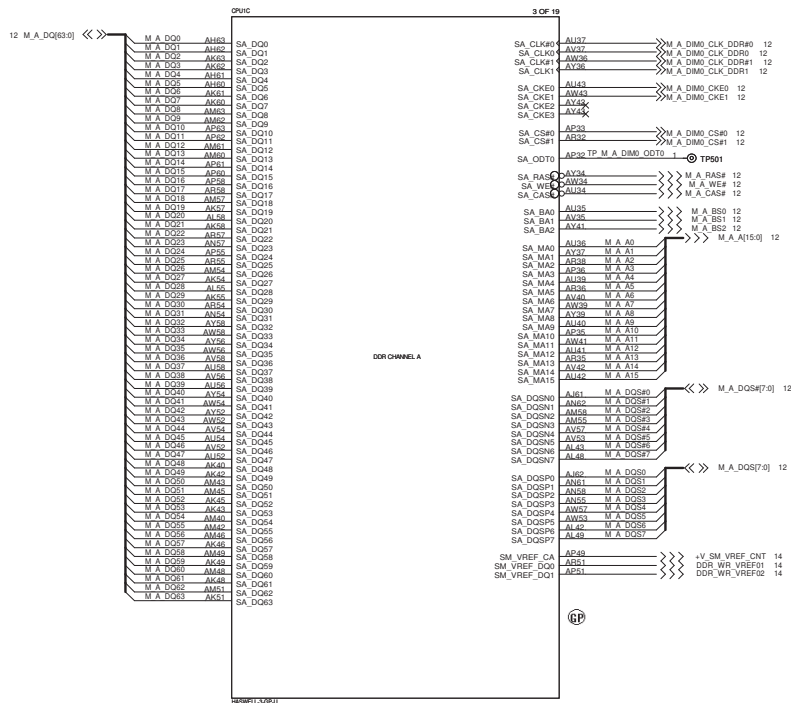
Wistron Corporation		
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File	Block Diagram	Rev
A2	Document Number	X00
Round Rock 13.3" UMA		
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	5	4	3	2	1
D					
C					
B					
A					

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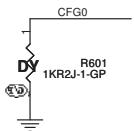
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		CPU (PCIE/DMI/FDI)	
Size A4	Document Number		Rev X00
Date: Friday, June 28, 2013		Sheet 3 of	107

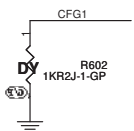


SSID = CPU

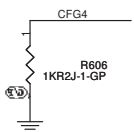
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0: Lane Reversed 1: (Default) Normal Operation; No stall



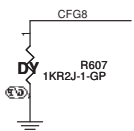
PCH/PCH LESS MODE SELECTION	
CFG1	0: Lane Reversed 1: (Default) Normal Operation



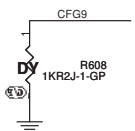
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



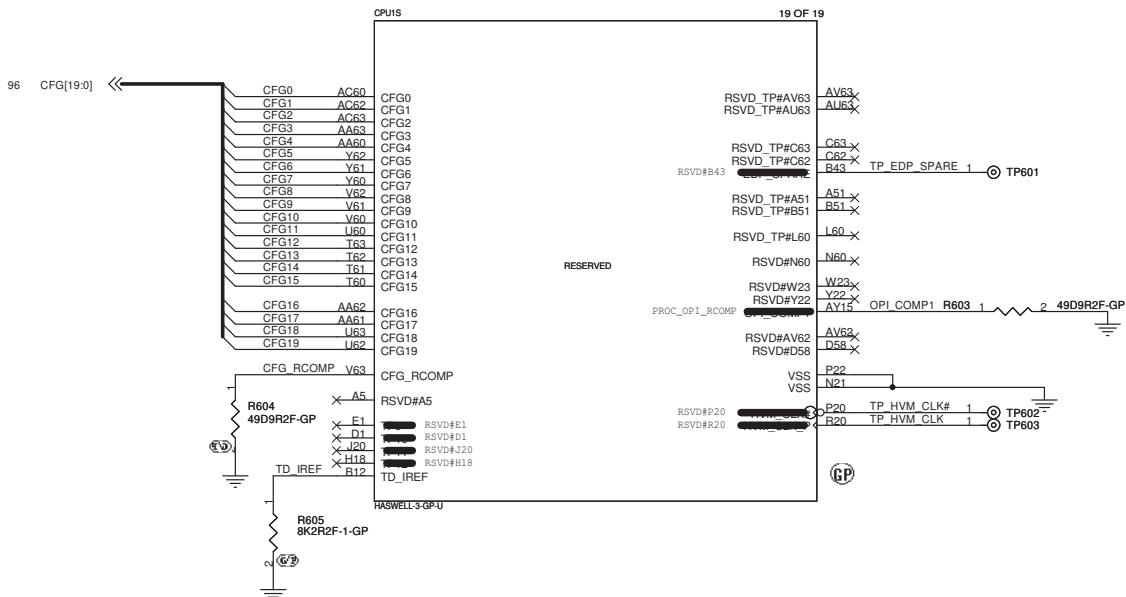
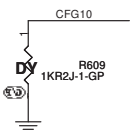
ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available peggardless of the locking of the unit



NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0: No VR support SVID is present The chip will not generate (OR Respond to) SVID activity



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



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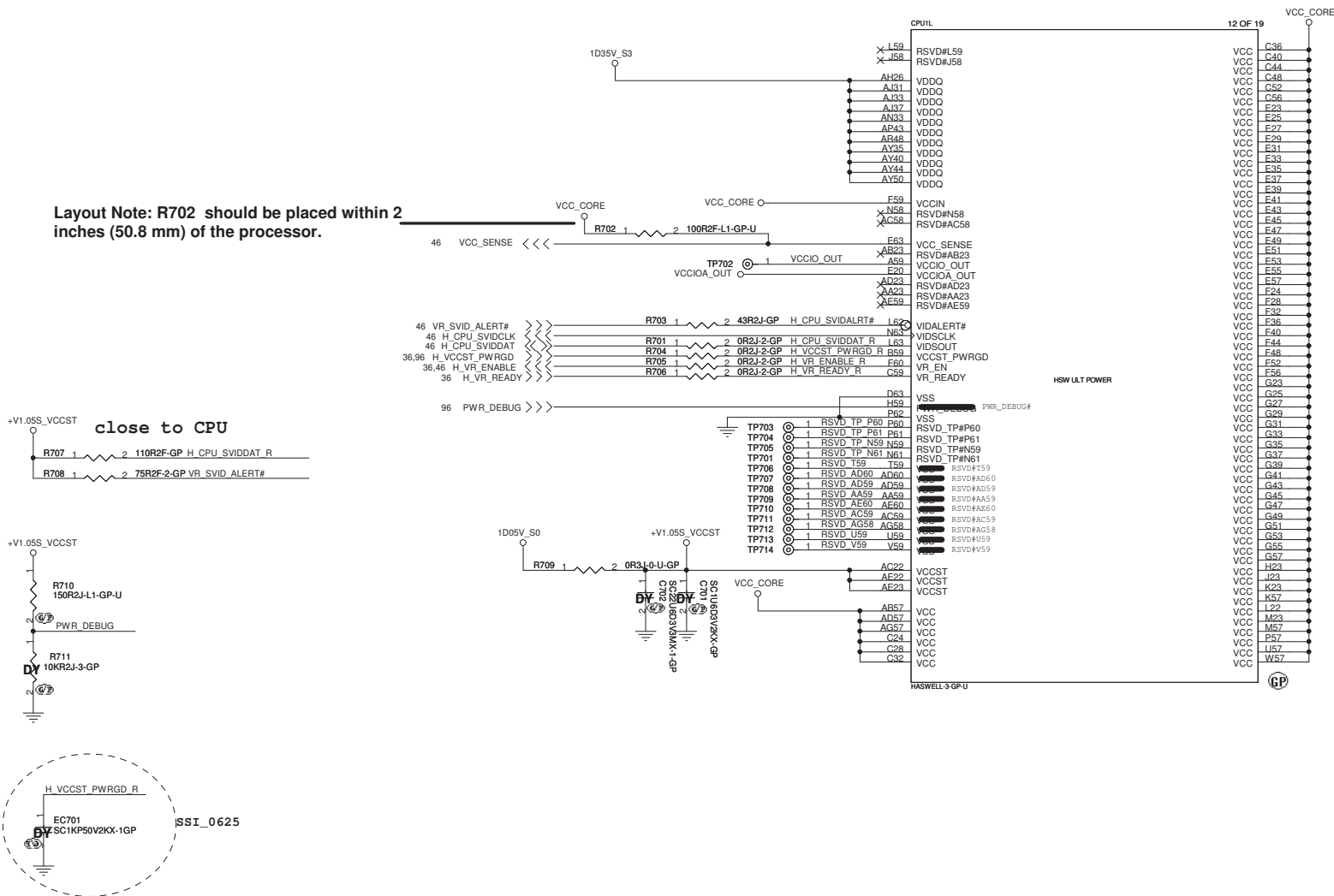
Title: **CPU (RESERVED)**

Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

Date: Friday, June 28, 2013 Sheet: 6 of 107

SSID = CPU

Layout Note: R702 should be placed within 2 inches (50.8 mm) of the processor.



<Core Design>



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Title

CPU (VCC_CORE)

Size	Document Number
Custom	

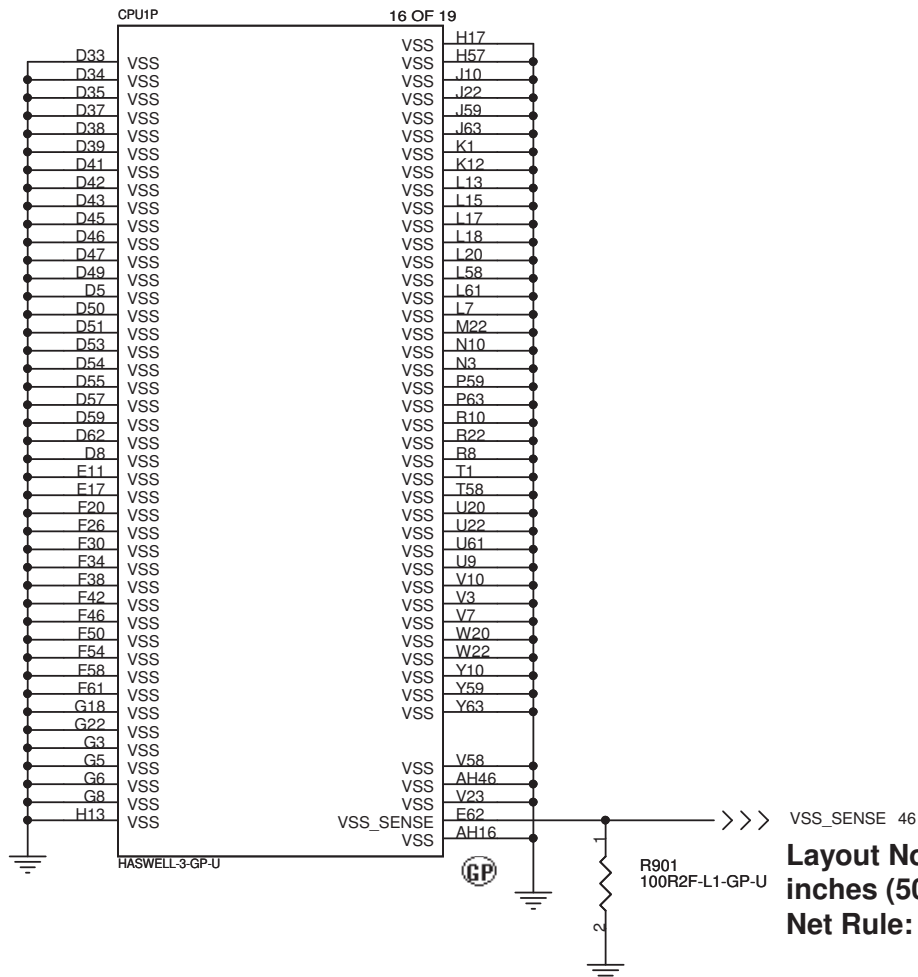
Round Rock 13.3" UMA

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Date: Friday, June 28, 2013 Sheet 7 of 107

SSID = CPU



Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals

<Core Design>



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Title

CPU (VSS)

Size
A4

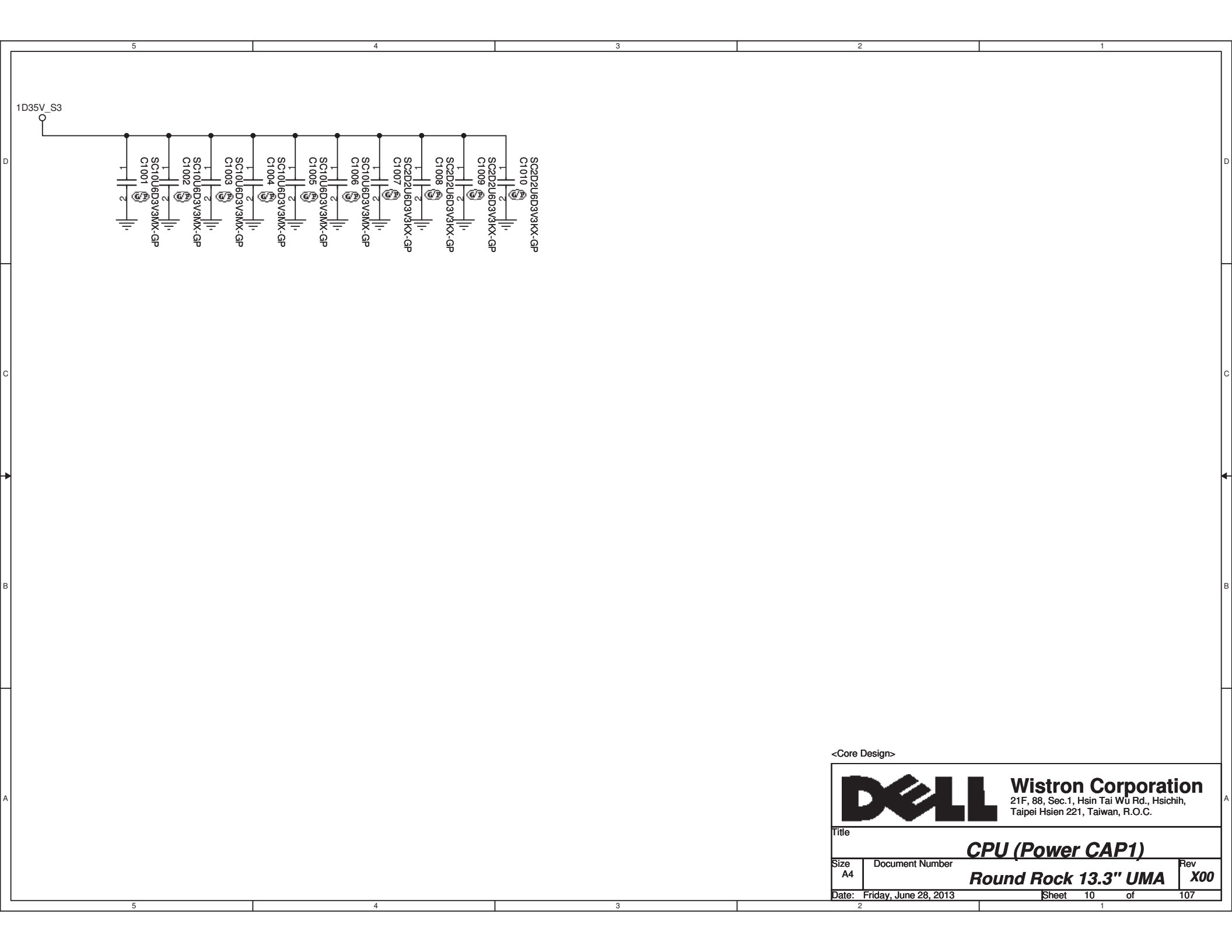
Document Number

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<Core Design>



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Title

CPU (Power CAP1)

Size
A4

Document Number

Rev
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Title

CPU (Power CAP2)

Size
A

Document Number

Round Rock 13.3" UMA

Rev

X00

Date: Friday, June 28, 2013

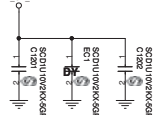
Sheet 11 of 107

SSID = MEMOR

Layout Note

Place these caps close to VREF_CAP

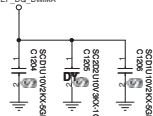
M VREF CA DIMMA



Layout Note

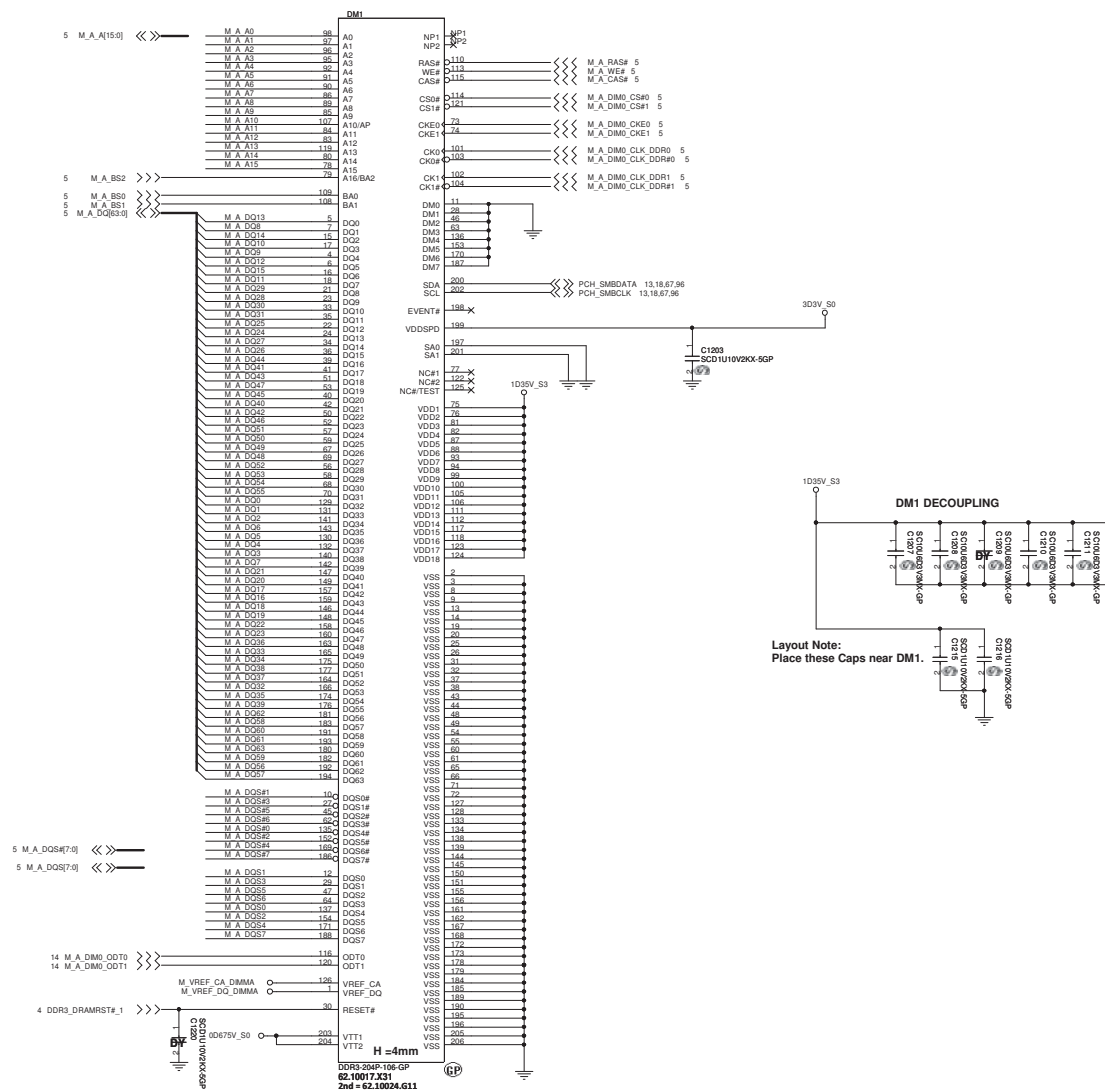
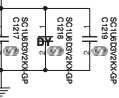
Place these caps close to VREF_DC

MVBFF DO DIMM



0D675V_S

**Place these caps
close to VTT1 and VTT2.**

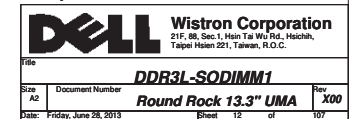


Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note:
Place these Caps near DM1.

<Core Design>



SSID = MEMORY

Layout Note:

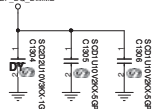
Place these caps close to VREF_CAP

M VREF CA DIMME



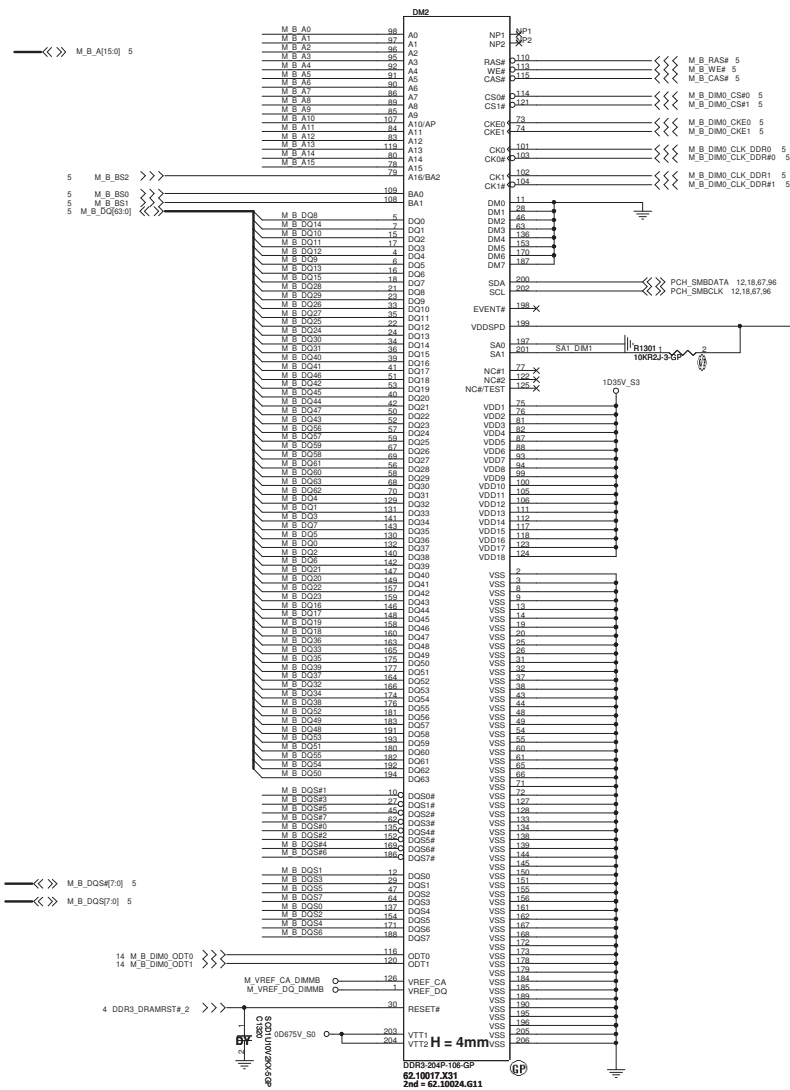
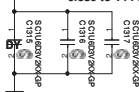
Layout Note

M VREF DQ DIMM



0D675V_S0

Place these caps
close to VTT1 and VTT2



Note:
SO-DIMMB SPD Address is 0xA
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

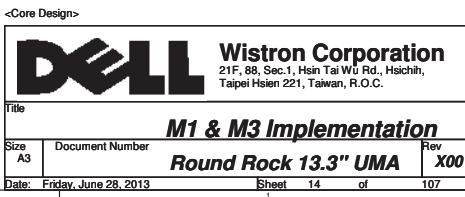
Layout Not
Place these



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Title			
DDR3L-SODIMM1			
Size A2	Document Number		Rev
	Round Rock 13.3" UMA		X00
Author	Editor	Version	Date

SSID = MEMORY

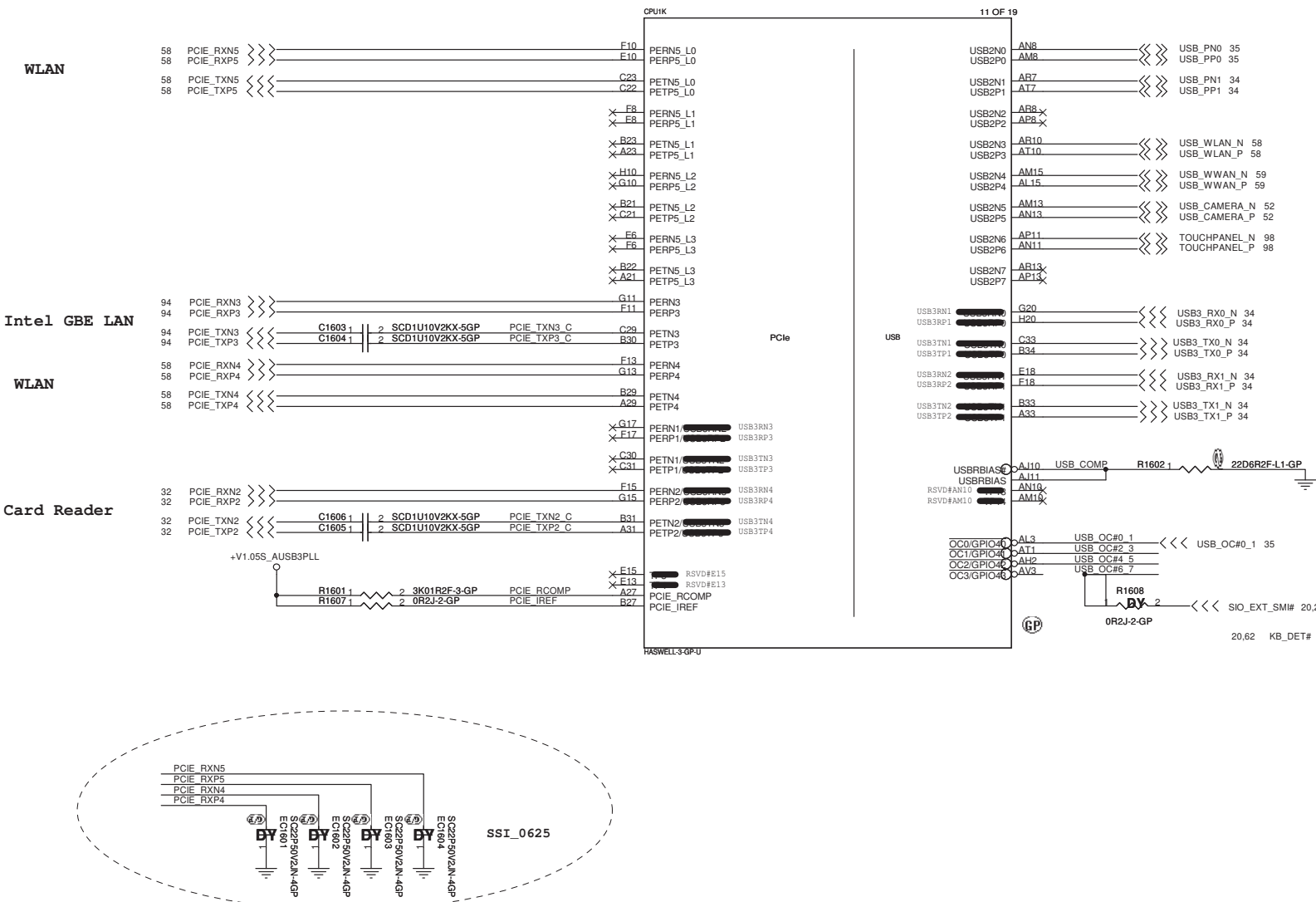


SSID = PCH

USB2.0 Table	
Pair	Device
0	USB port 2 (usb charger)
1	USB port 1 (win debug)
2	N/A
3	WLAN (BT)
4	WWAN
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 Table	
Pair	Device
1	USB port 1
2	USB port 2
3	N/A
4	N/A

Shark Bay ULT:
USB Ext. port 1
External debug port use on Shark Bay platform



<Core Design>

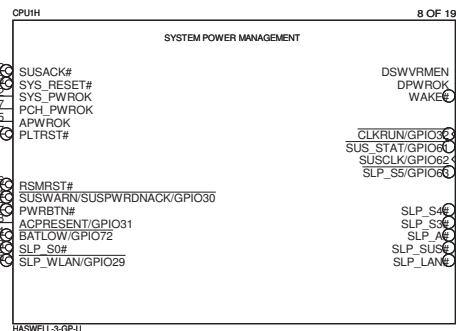
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Title: **CPU (PCIE/USB)**

Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

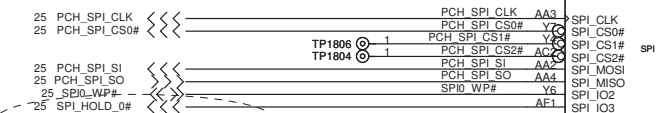
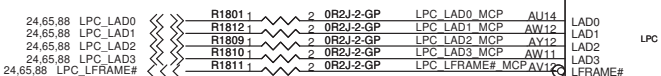
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NOTE:
PWRBTN# Integrated Pull-Up.

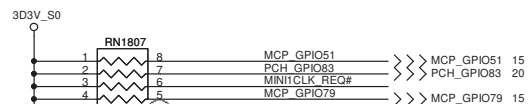


PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

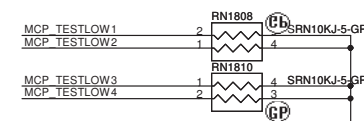
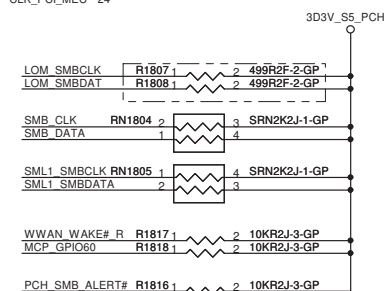
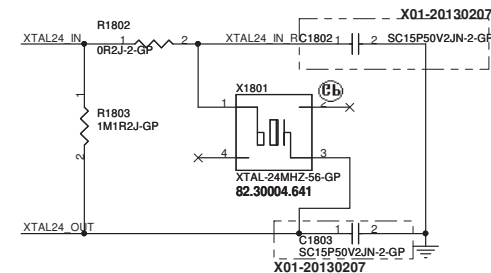
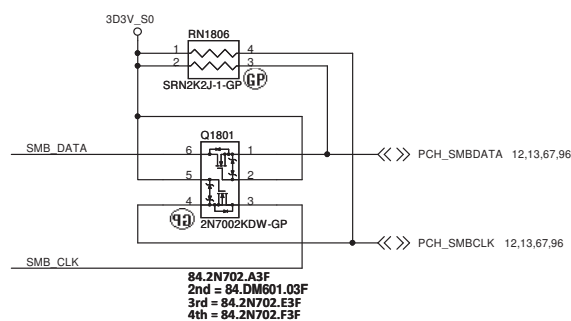
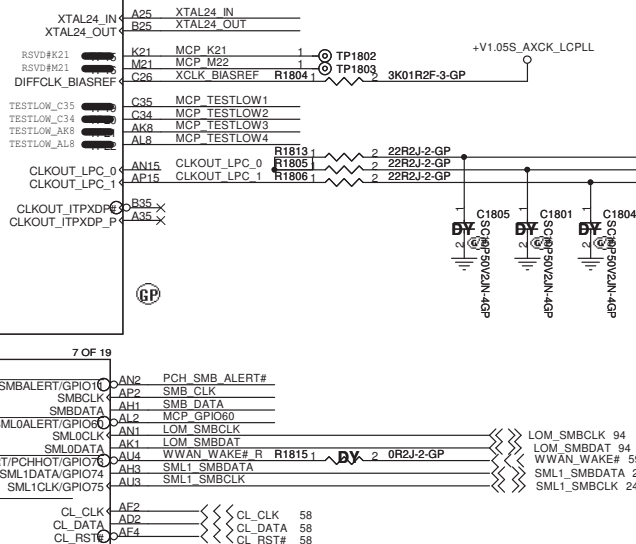
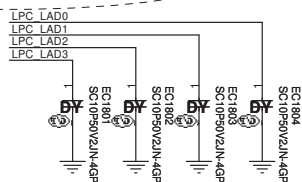
CPU#1				
X	C43	CLKOUT PCIE_N0		
X	C42	CLKOUT PCIE_P0		
X	U0	PCIECLKRQ0/GPIO18		
N	B41	CLKOUT PCIE_N1		
P	A41	CLKOUT PCIE_P1		PCIE Port 2
	U0	PCIECLKRQ1/GPIO19		
N	B42	CLKOUT PCIE_N2		
P	C41	CLKOUT PCIE_P2		CLK SIGNALS
	A00	PCIECLKRQ2/GPIO20		PCIE Port 3
N	B38	CLKOUT PCIE_N3		
P	C37	CLKOUT PCIE_P3		
	M0	PCIECLKRQ3/GPIO21		PCIE Port 4
N	A39	CLKOUT PCIE_N4		
P	B39	CLKOUT PCIE_P4		
	U0	PCIECLKRQ4/GPIO22		PCIE Port 5
N	B37	CLKOUT PCIE_N5		
P	A37	CLKOUT PCIE_P5		
	U0	PCIECLKRQ5/GPIO23		PCIE Port 6



SSSI 0618



SSI_0625



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Title	CPU (CLOCK/SMBUS/CL/LPC/SPI)
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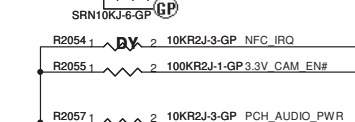
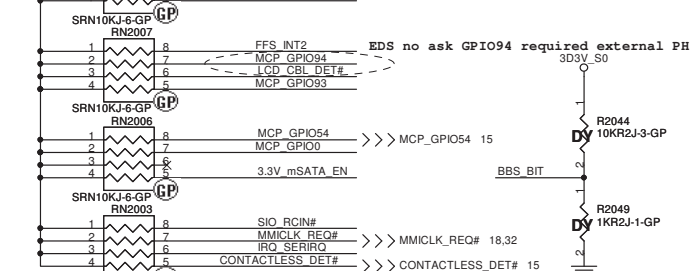
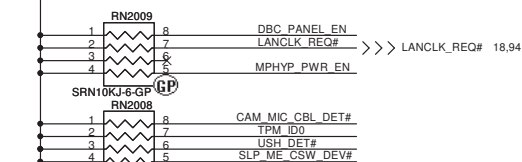
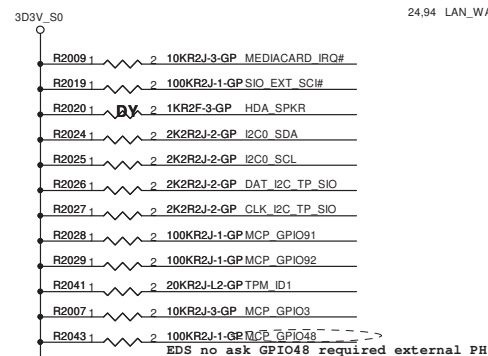
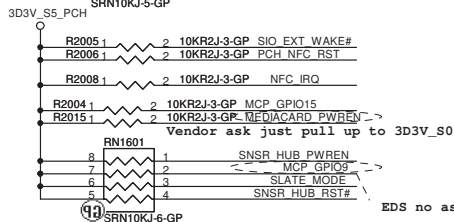
Size A3	Document Number Round Rock 13.3" UMA	Rev X00
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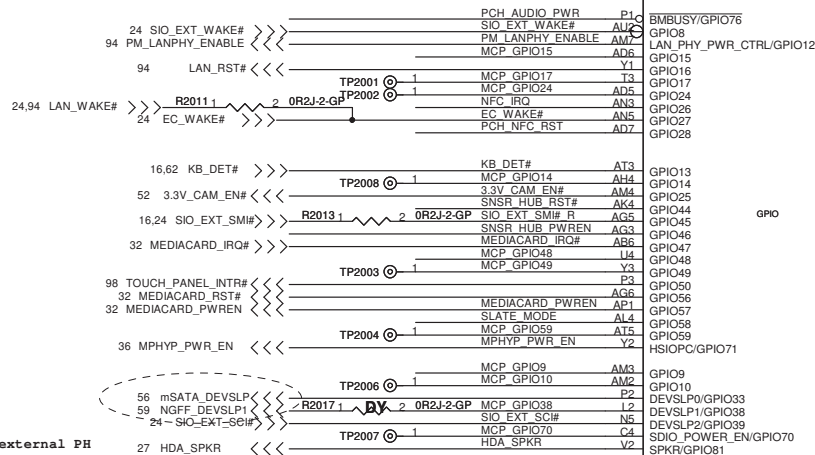
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		Wistron Corporation 21F, 86, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title			
CPU (RTC/SATA/HDA/JTAG)			
Size A3	Document Number	Round Rock 13.3" UMA	
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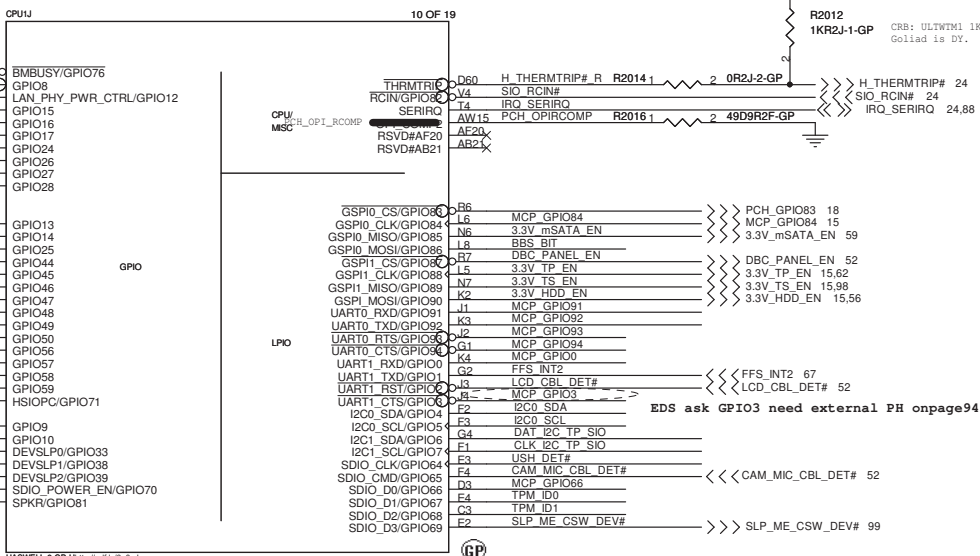
SSID = PCH



EDS no ask GPIO9 required external PH



No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot



EDS ask GPIO3 need external PH on page 94

<http://adf.ly/3o8pJ>

BOOT BIOS Strap	
GPIO86	BOOT BIOS Location
0	SPI (Default)
1	LPC

TOP-BLOCK SWAP OVERRIDE	
GPIO66	
HIGH pop R20545	
LOW pop R2051 (DEFAULT)	

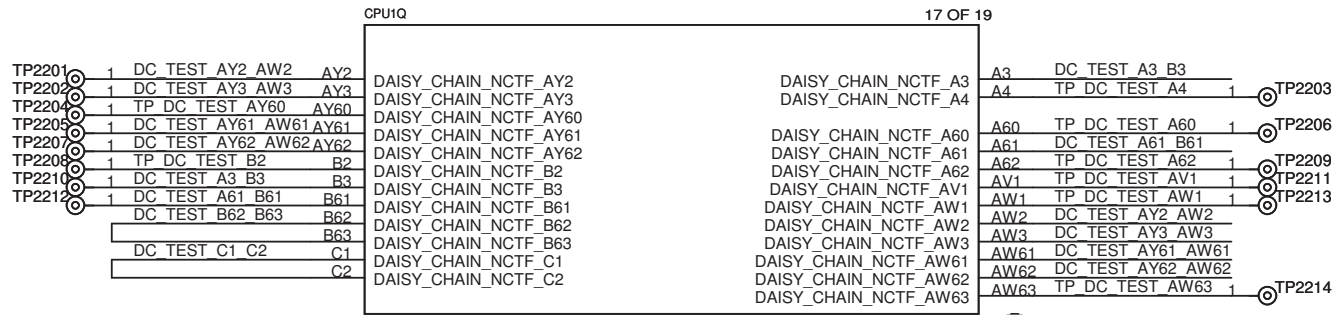
<Core Design>

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Title: **CPU (GPIO/CPU)**

Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

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<Core Design>



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Title

CPU (RSVD)

Size
A4

Document Number

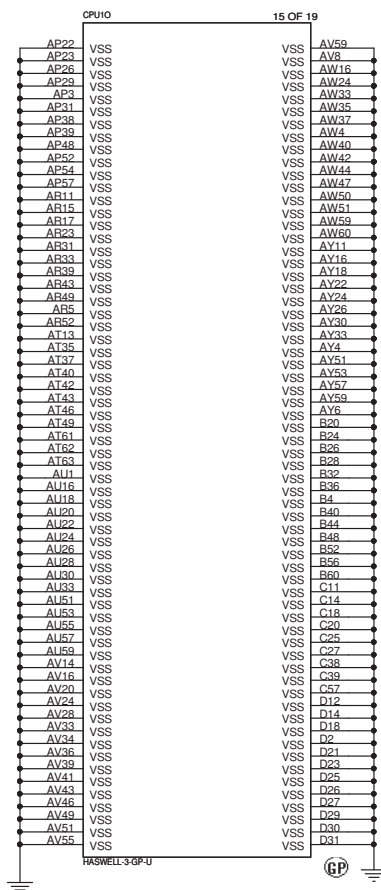
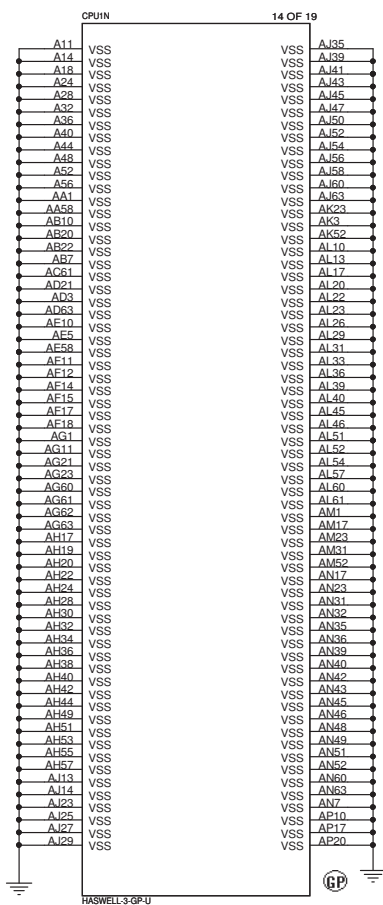
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SSID = PCH



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Title

CPU (VSS)

Size

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SSID = KBC

303V SS

R2401 1 2 0R2J-2-GP

R2402 1 2 0R2J-2-GP

VTR ADC

X01-20130222

L2017 1 2 1M27045121AT-GP

C2407

SCD1U10V2KX-GP

C2408

SC1U4D75V2KX-GP

U2401

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B410

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B412

B413

B414

B415

B416

B417

B418

B419

B420

B421

B422

B423

B424

B425

B426

B427

B428

B429

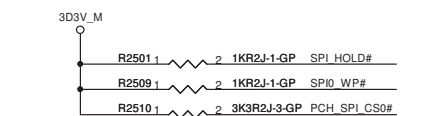
B430

B431

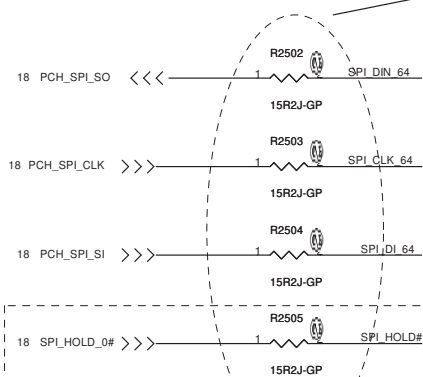
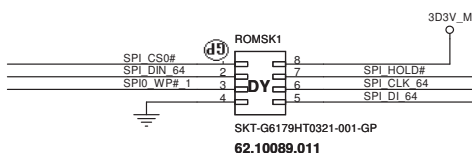
B432

SSID = Flash.ROM

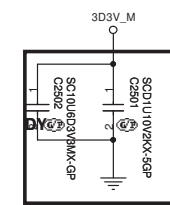
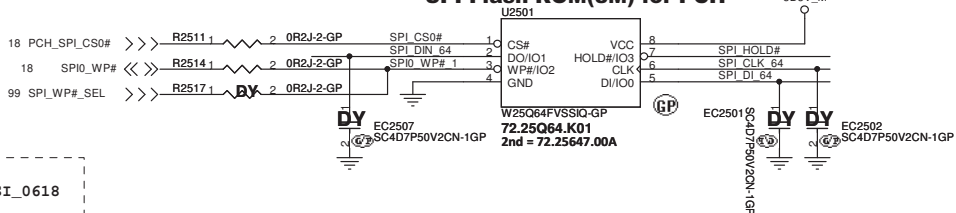
SPI ROM Equal length need to less than 500mil



Schematic Design Checklist
Single Device: 15
Multiple Devices: 33 per branch

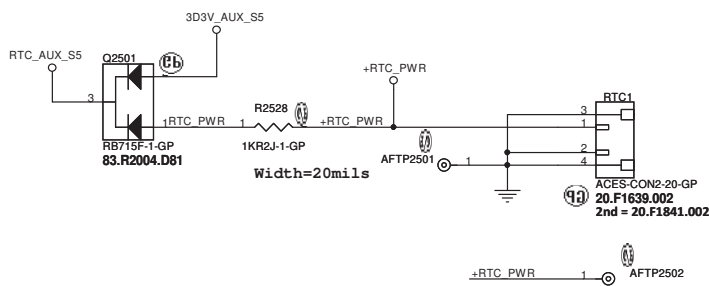


SYSTEM SPI ROM
SPI Flash ROM(8M) for PCH



Layout Note: Close to U2501 Pin 8

SSID = RTC



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

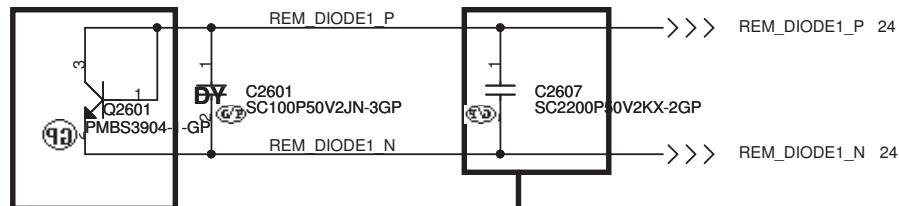
Title: **Flash/RTC**

Size: A3 Document Number: **Round Rock 13.3" UMAX00** Rev

Date: Friday, June 28, 2013 Sheet 25 of 107

SSID = Thermal

84.03904.L06
2ND = 84.03904.P11

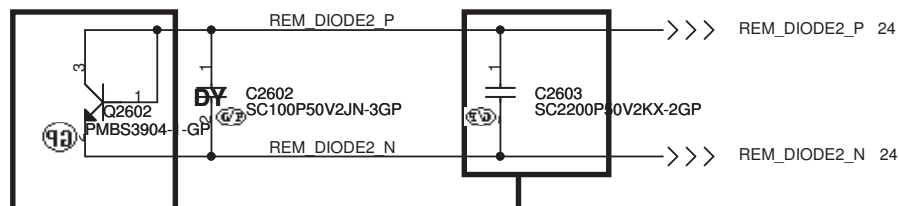


Layout Note: Place to CPU

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

84.03904.L06
2ND = 84.03904.P11

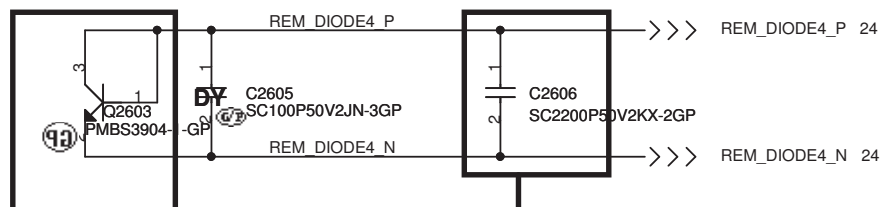


Layout Note: Place to DIMM

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

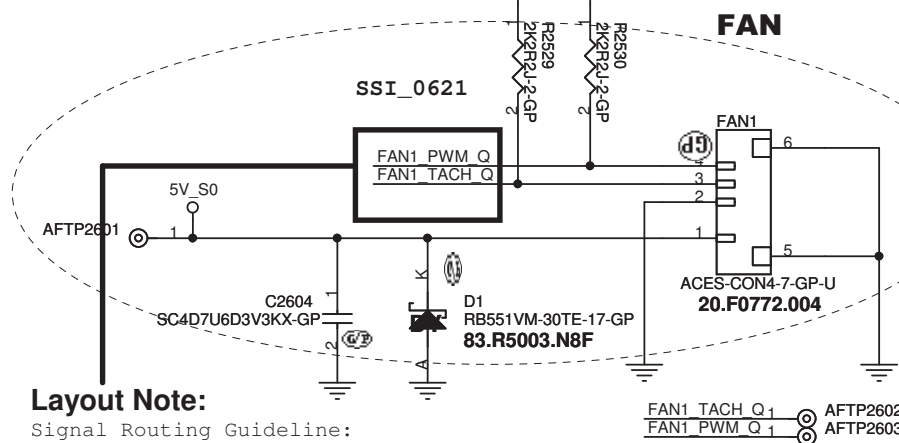
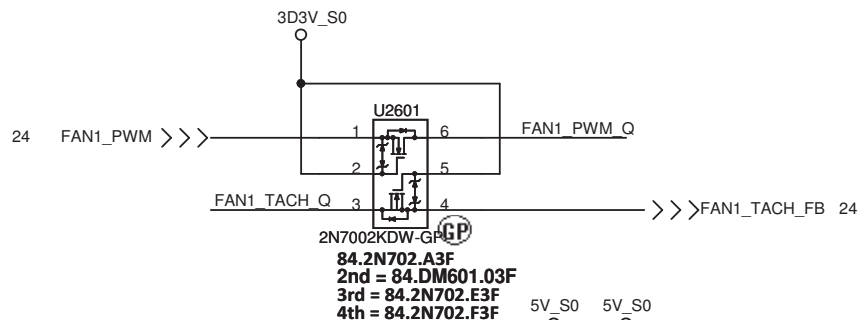
84.03904.L06
2ND = 84.03904.P11



Layout Note: Place to V.R

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC



Layout Note:

Signal Routing Guideline:
Trace width = 15mil

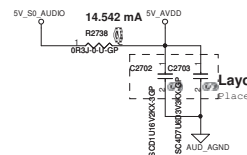
<Core Design>



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Title Thermal/Fan		
Size A4	Document Number Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013	Sheet 26 of 107	

SSID = AUDIO



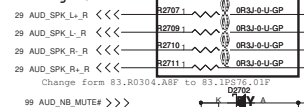
Layout Note:
Place close to Pin 26



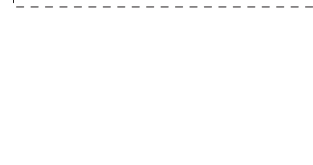
Layout Note:

trace width=30mil
R2707,R2709,R2710,R2711 near CODEC

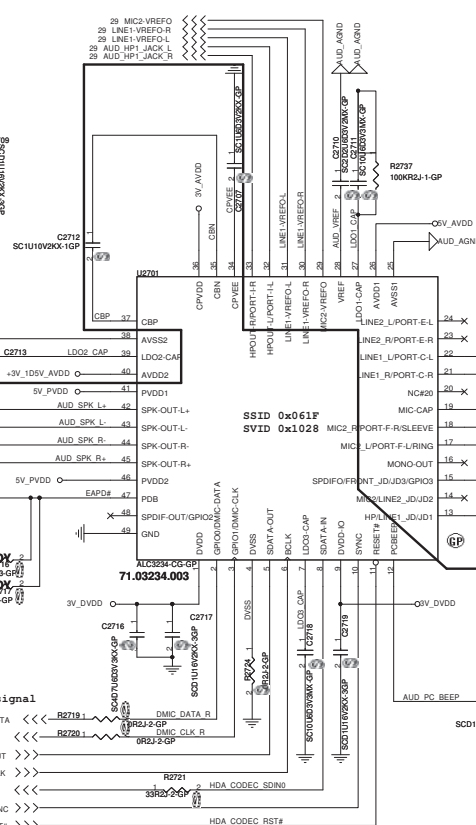
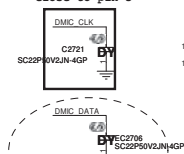
Analog
Digital



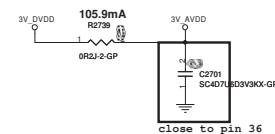
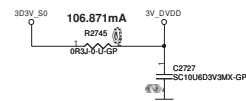
Change form 83.R0304.A8F to 83.1PS76.01F



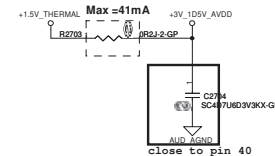
DMIC: > 5mil and keep out the analog signal
close to pin 3



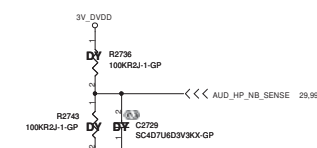
```
SSID 0x061F
SVID 0x1028
```



close to pin 36

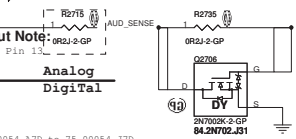


AUD AGND
close to pin 40

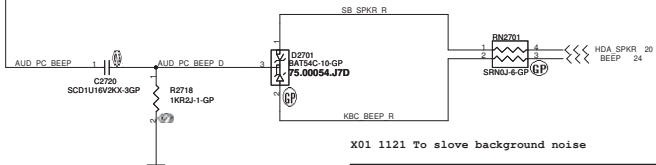


Layout Note: OR

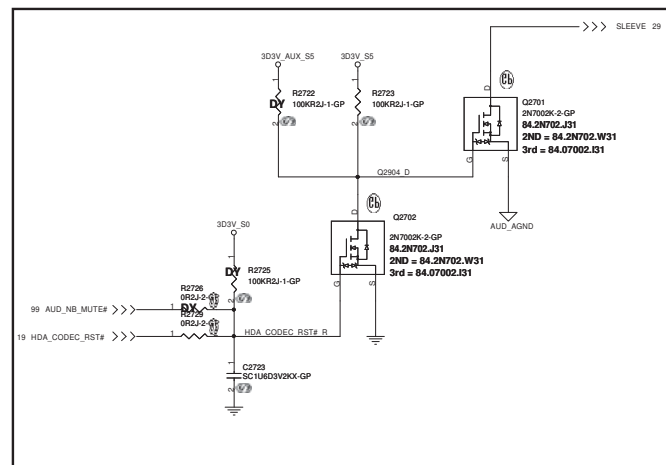
Ana



Change form 75.00054.A7D to 75.00054.J7D



X01 1121 To slove background noise



Core Design:

DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Codec ALC3234
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(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A

Document Number

Round Rock 13.3" UMA

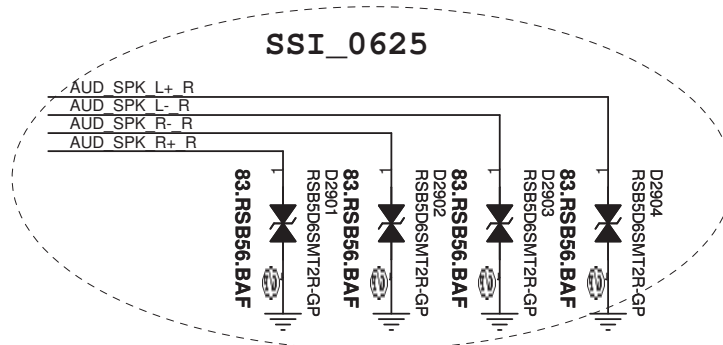
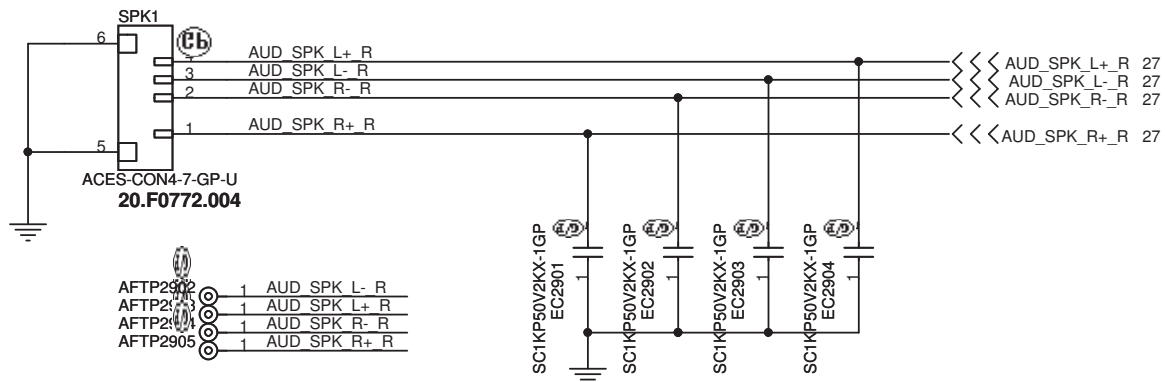
Rev
X00

Date: Friday, June 28, 2013

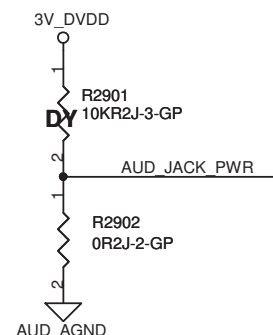
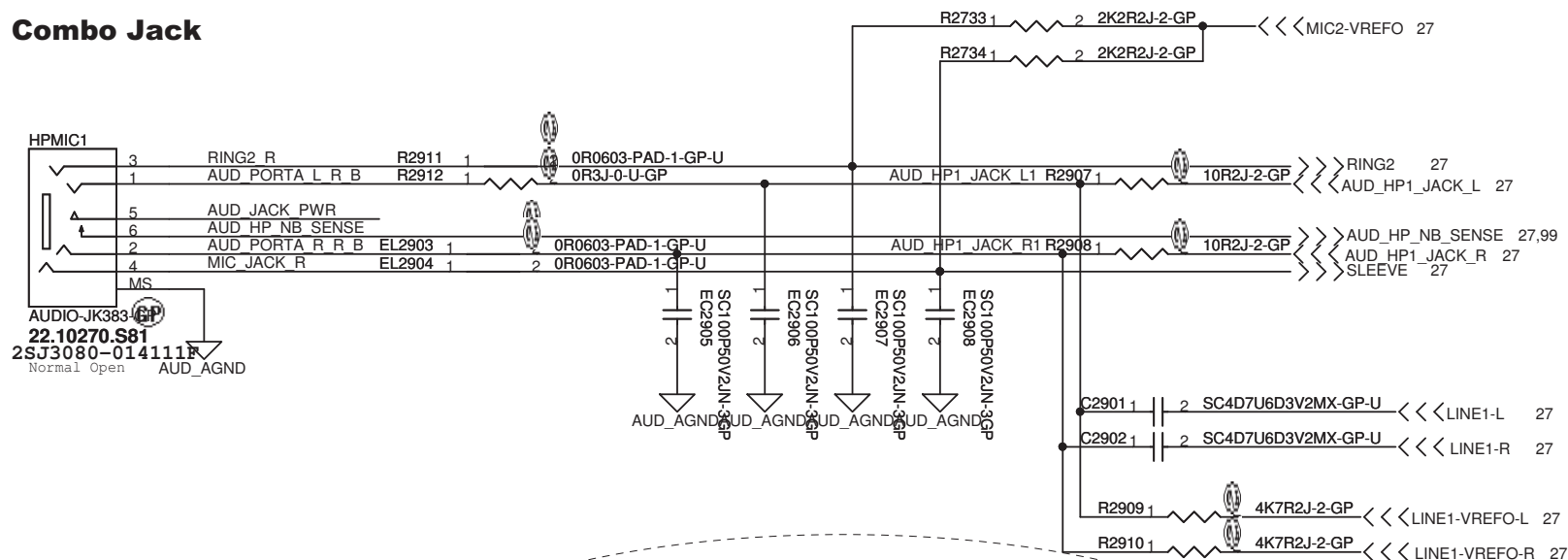
Sheet 28 of 107

SSID = AUDIO

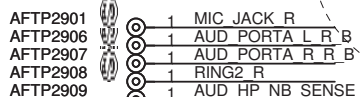
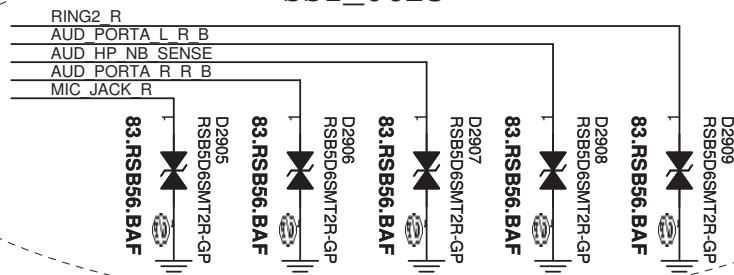
Speaker 2W/ch



Combo Jack



SSI_0625



<Core Design>



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Title

Speaker/HPMIC CONN

Size

Document Number

A4

Round Rock 13.3" UMA

Rev

X00

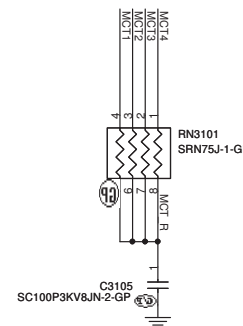
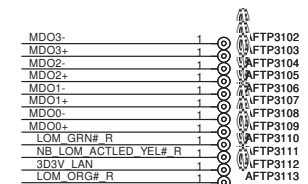
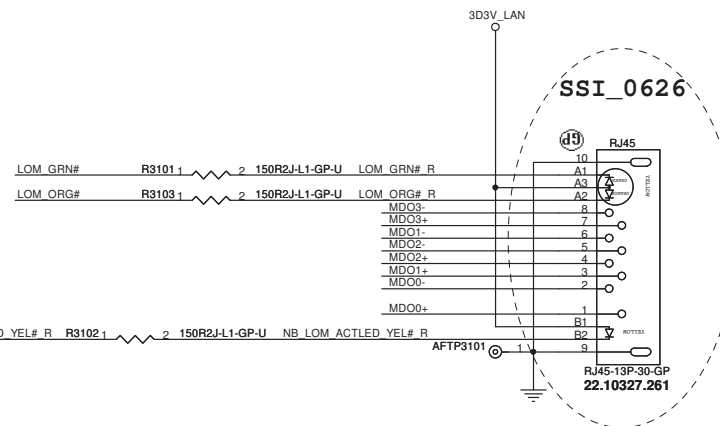
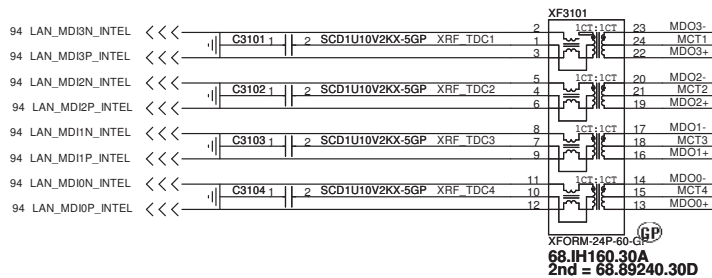
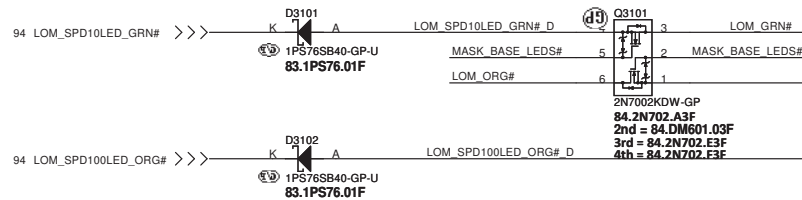
Date: Friday, June 28, 2013

Sheet 29

of

107

SSID = LOM



<Core Design>

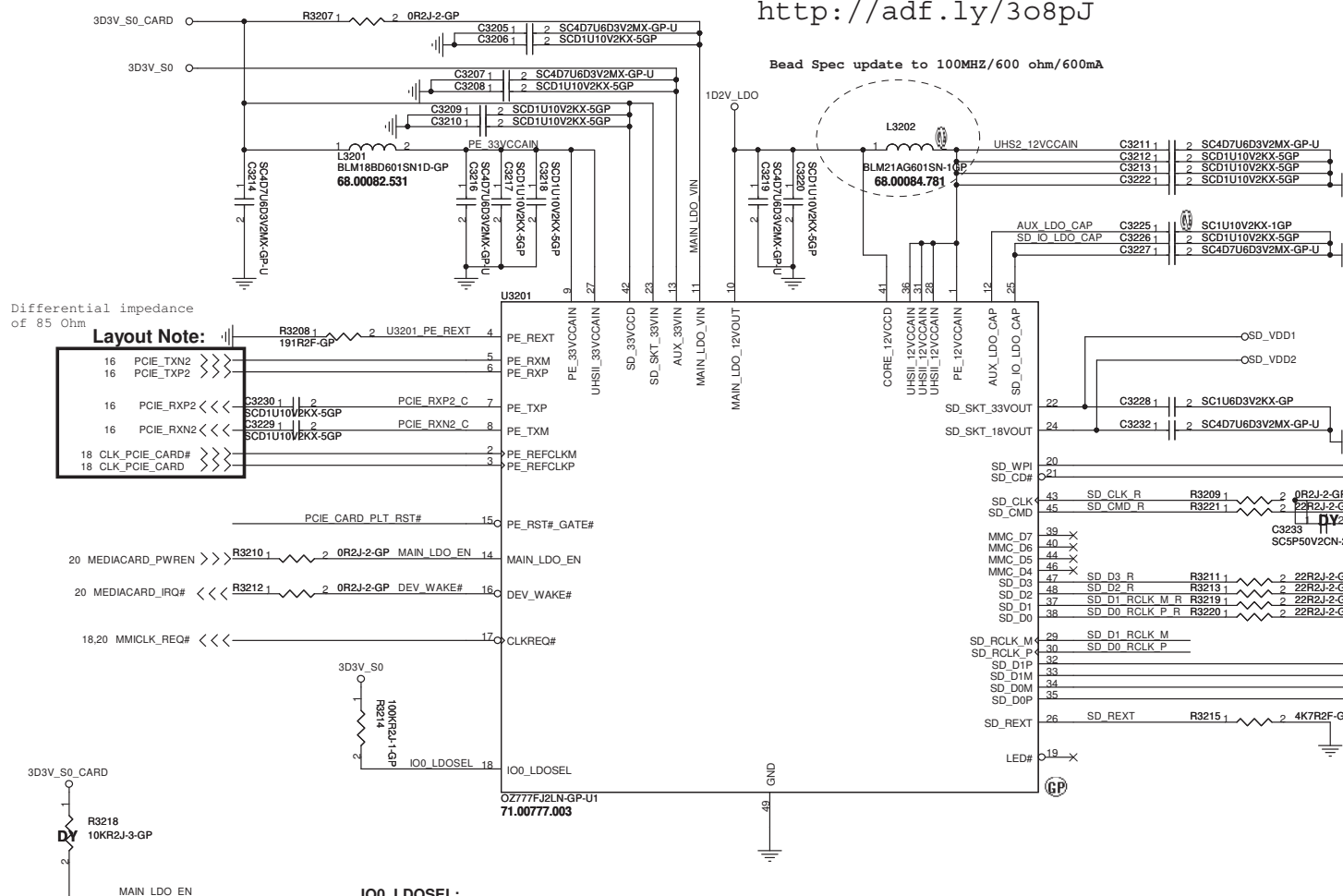
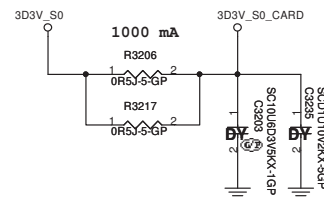
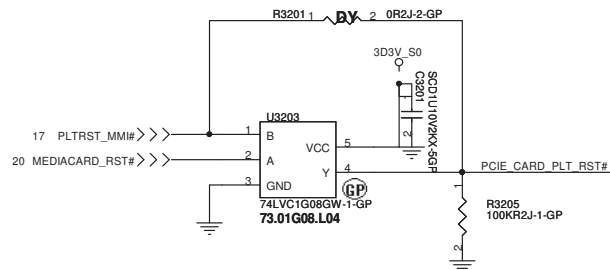
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 Taipei Hsien 221, Taiwan, R.O.C.

Title **RJ45/Transformer**

Size A3 Document Number **Round Rock 13.3" UM100** Rev

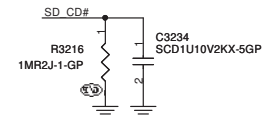
Date: Friday, June 28, 2013 Sheet 31 of 107

SSID =Card Reader



<http://adf.ly/3o8pJ>

Bead Spec update to 100MHZ/600 ohm/600mA

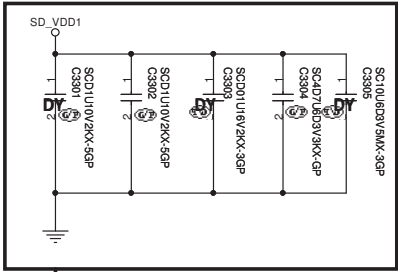


add one more pull down 1Mohm resistor on SD_CD# for the OZ777FJ2LN-A.
For the OZ777FJ2LN-B, you can remove these 1Mohm resistor and 0.1uF capacitor.

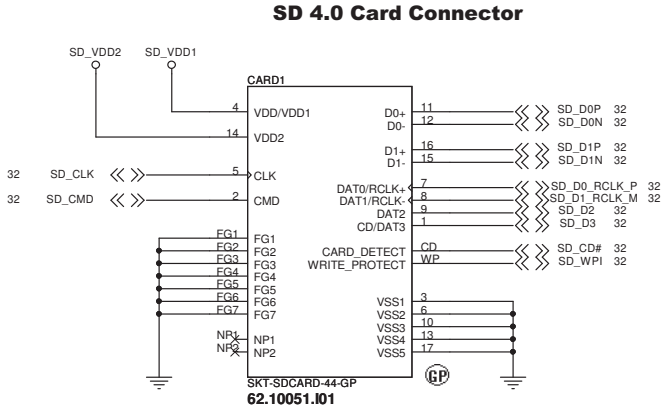
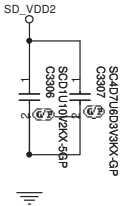
For UHS-II

IO0_LD0SEL:
High means select internal LDO for main area core power.
Low means select external LDO for main area core power.

SSID =Card Reader

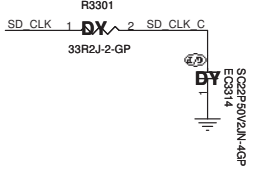
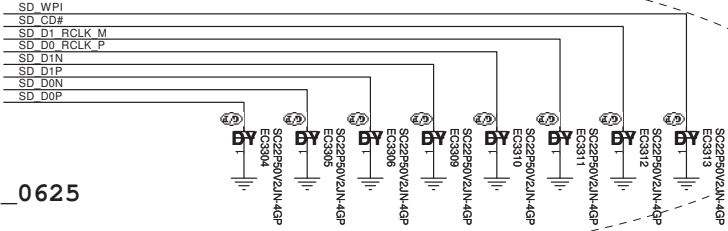


Layout Note:Close to Card Reader CONN



SD_CD#	1	AFTP3301
SD_D3	1	AFTP3302
SD_CLK	1	AFTP3303
SD_CMD	1	AFTP3304
SD_D0_RCLK_P	1	AFTP3305
SD_D1_RCLK_M	1	AFTP3306
SD_D2	1	AFTP3307
SD_WPI	1	AFTP3308
SD_VDD1	1	AFTP3309
SD_D0P	1	AFTP3311
SD_D0N	1	AFTP3312
SD_D1P	1	AFTP3313
SD_D1N	1	AFTP3310

SD_D3
SD_CMD
SD_D2



SSI_0625

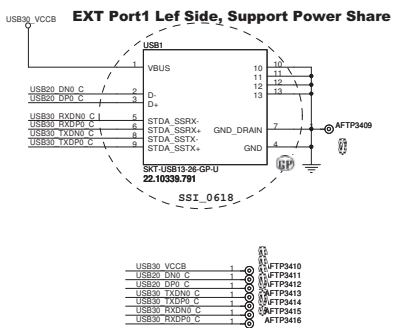
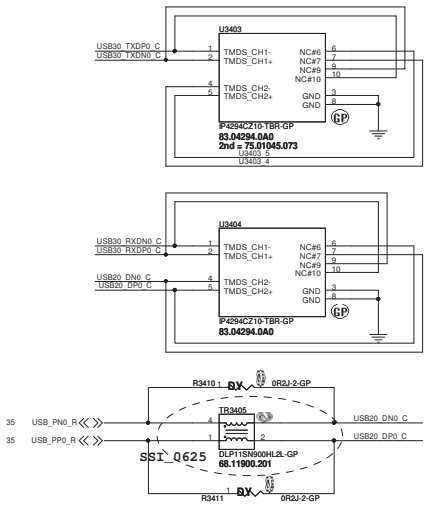
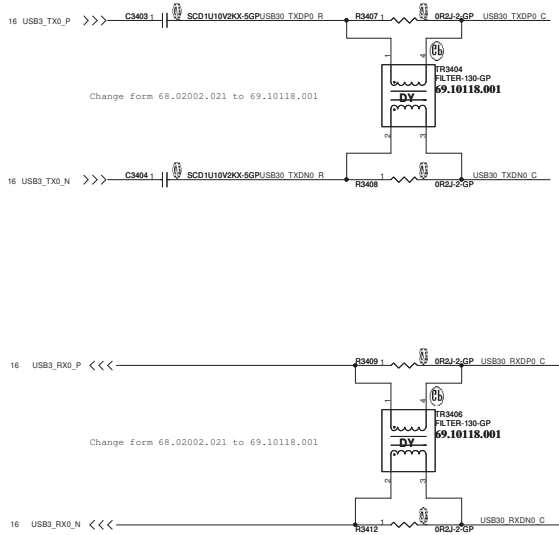
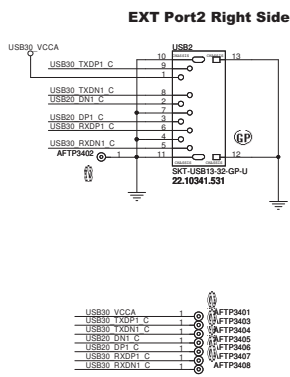
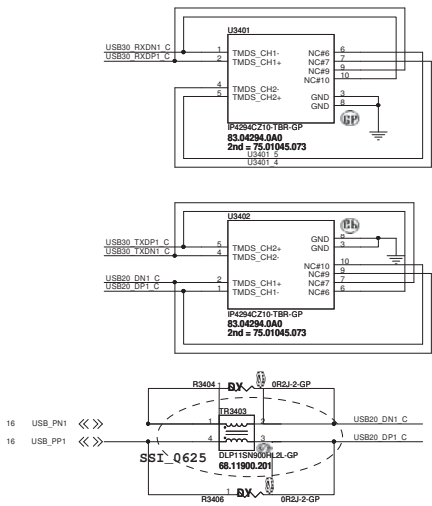
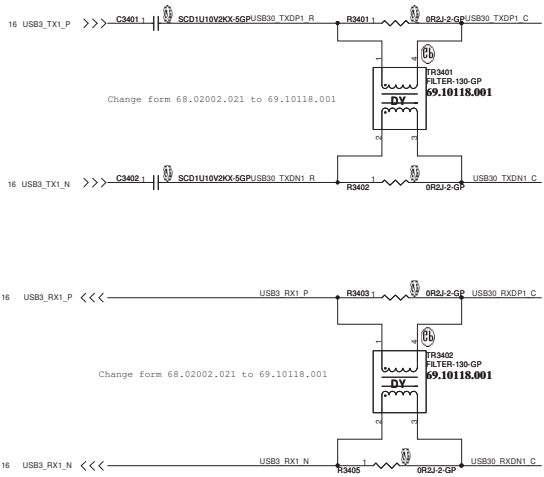
<Core Design>

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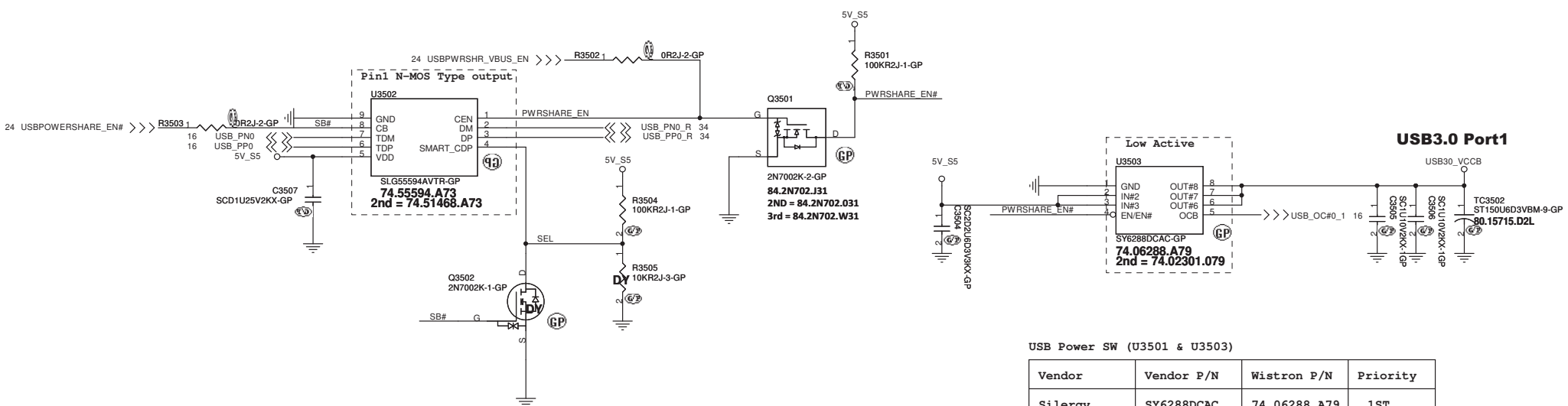
Title **Card Reader CONN**

Size A3	Document Number Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013	Sheet 33 of 107	

SSID = USB



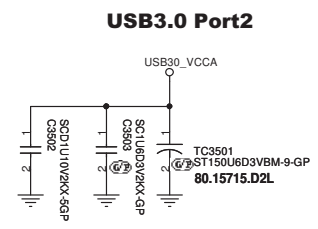
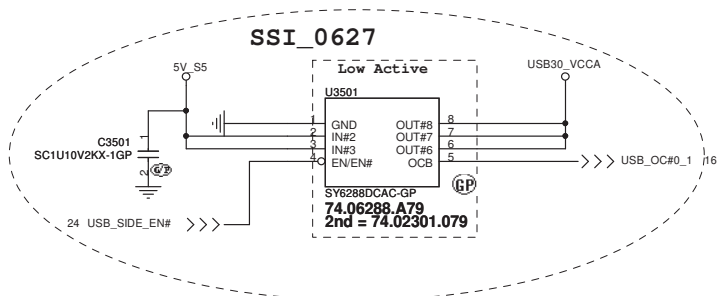
SSID = USB



Vinafix.com

USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND
			3RD



SSID = Reset.Suspend

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

S3 Reduction

Size
A4

Document Number

Round Rock 13.3" UMA


Rev
X00

Date: Friday, June 28, 2013

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number		Rev
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		Round Rock 13.3" UMA00	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Reserved		
Size A	Document Number Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013		Sheet 39 of 107

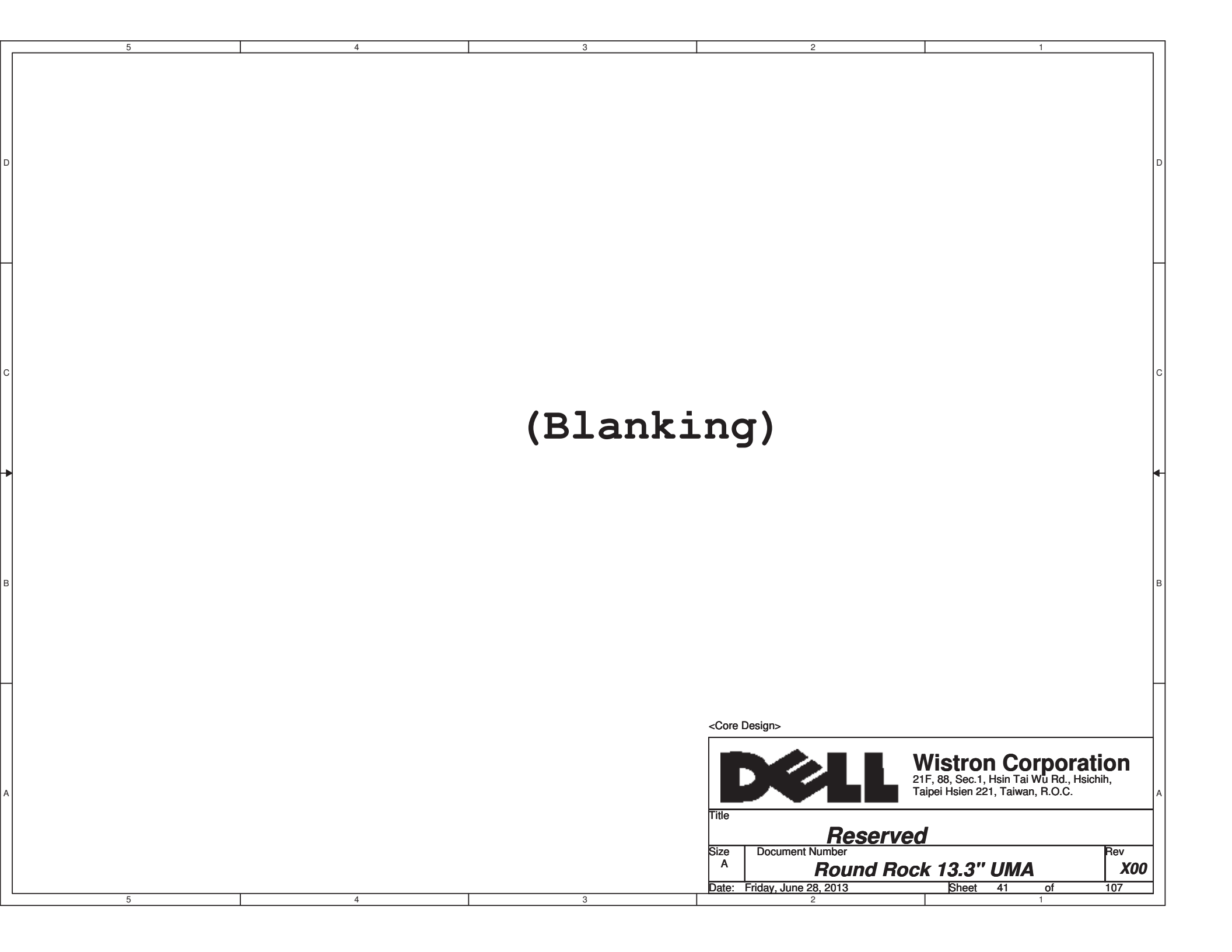
5 4 3 2 1

SSID = OBFF

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number		Rev X00
Date: Friday, June 28, 2013		Sheet 40 of	107

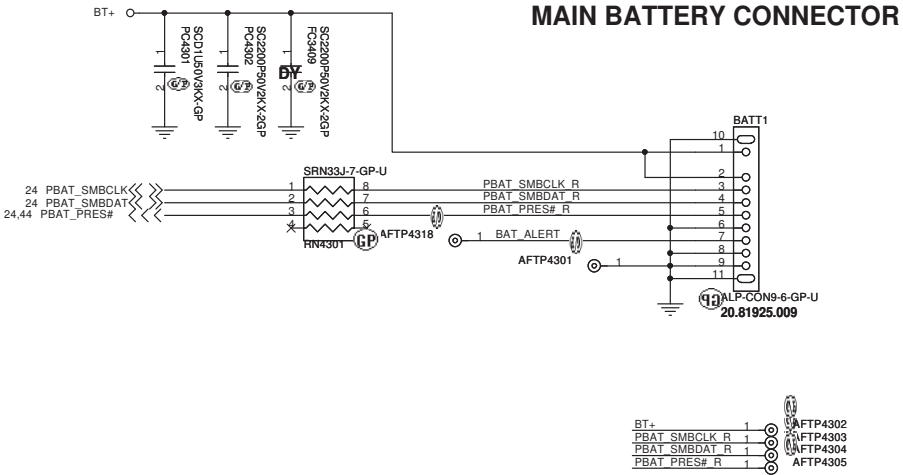


(Blanking)

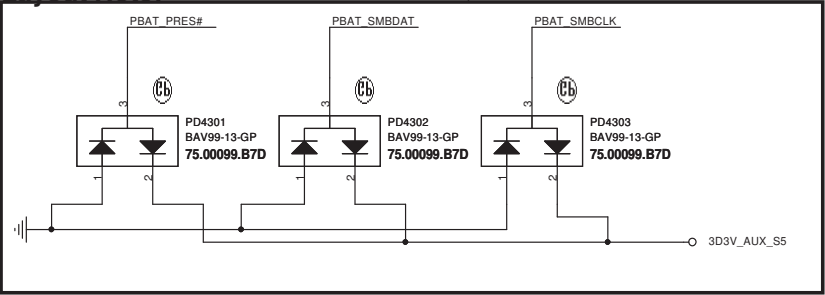
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A	Document Number Round Rock 13.3" UMA		Rev X00
Date: Friday, June 28, 2013		Sheet 41 of	107

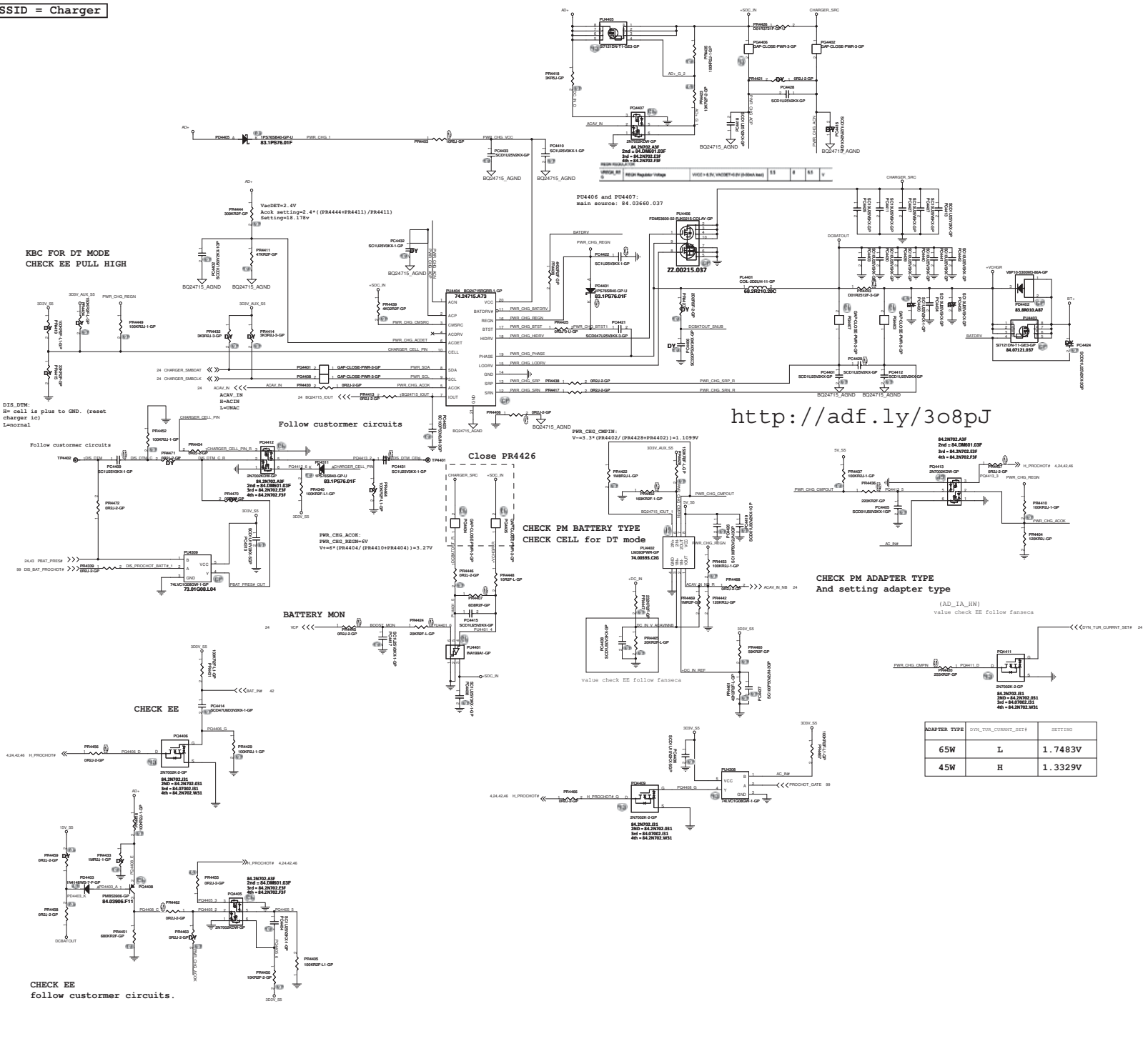
SSID = PWR.Support



Layout Note: Place near Battery CONN



SSID = Charger



<http://adf.ly/3o8pJ>

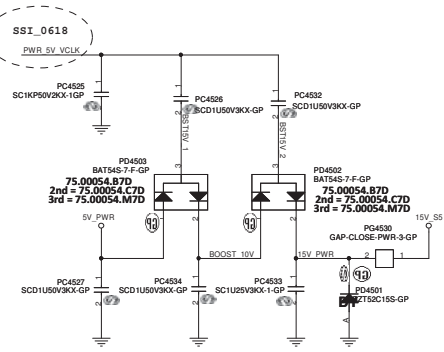
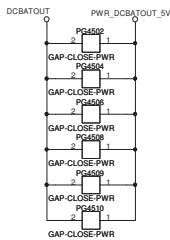
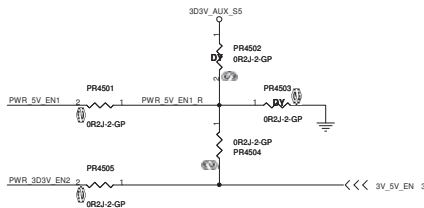
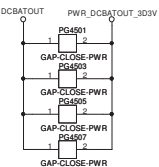
CHECK PM BATTERY TYPE
CHECK CELL for DT mode

CHECK PM ADAPTER TYPE
And setting adapter type

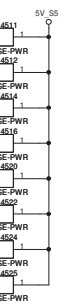
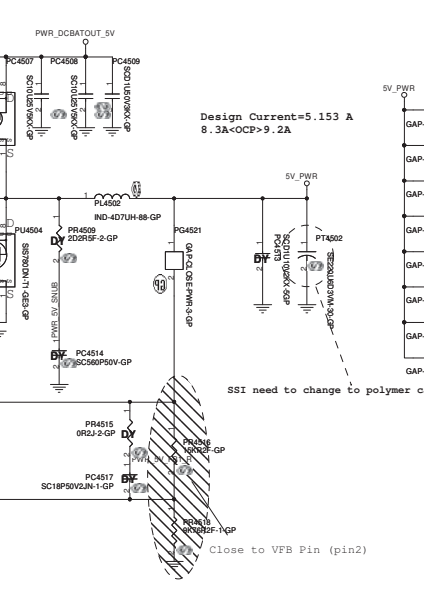
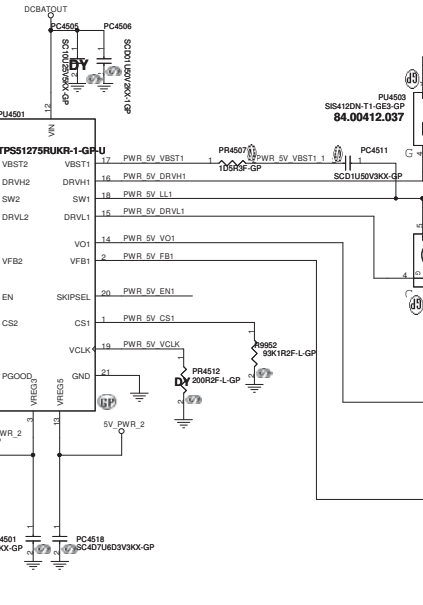
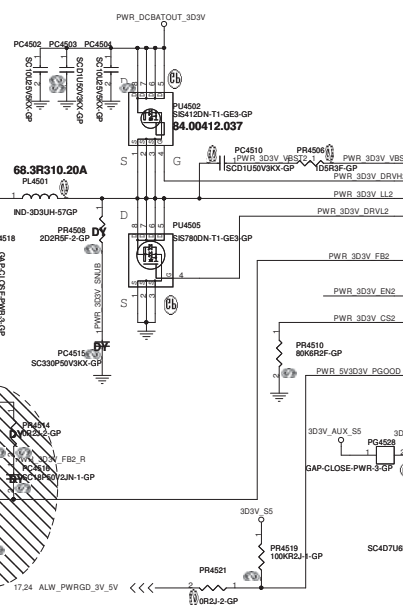
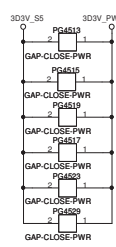
ADAPTER TYPE	DVL_TUR_CURRENT_SET#	SETTING
65W	L	1.7483V
45W	H	1.3329V

CHECK EE
follow customer circuits.

SSID = PWR.Plane.Regulator_5v3p3v



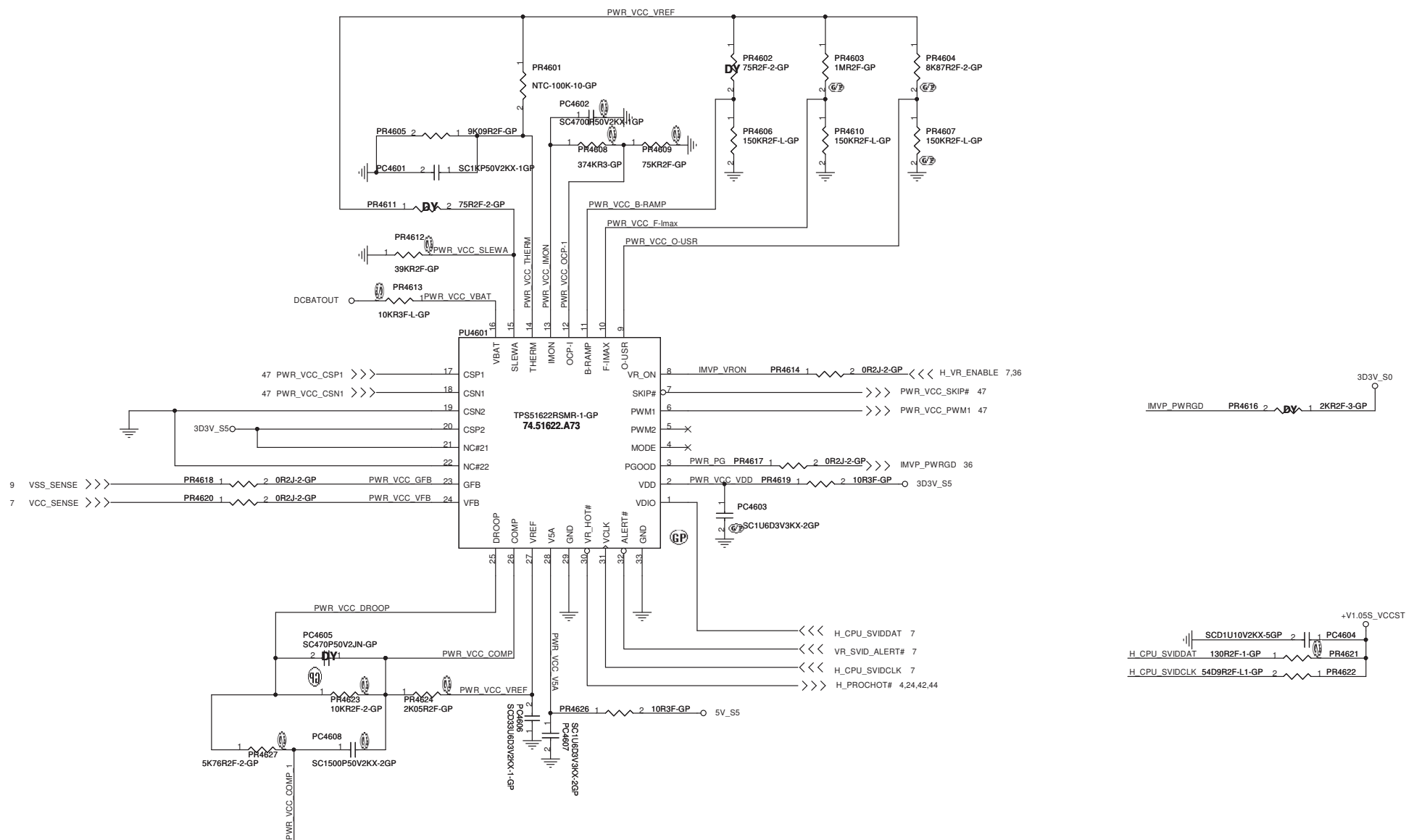
Design Current=5.894 A
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I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMO063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI5412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMO063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI5412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

```
SSID = CPU.Regulator
```



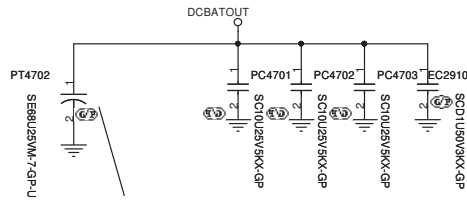
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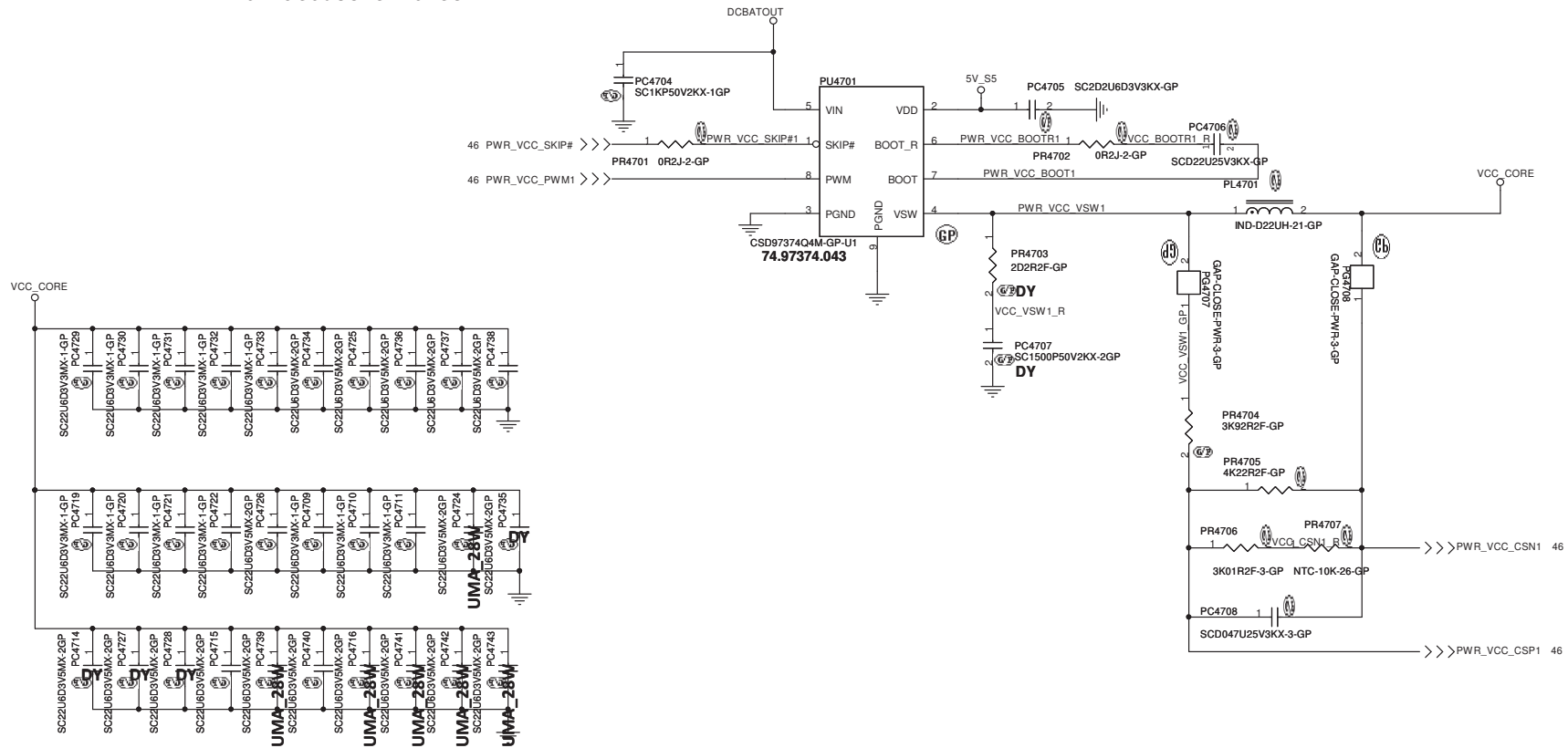
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
TPS51622 CPUCORE(1/2)			
Size	Document Number		Rev
A3		Round Rock 13.3" UMA	X00
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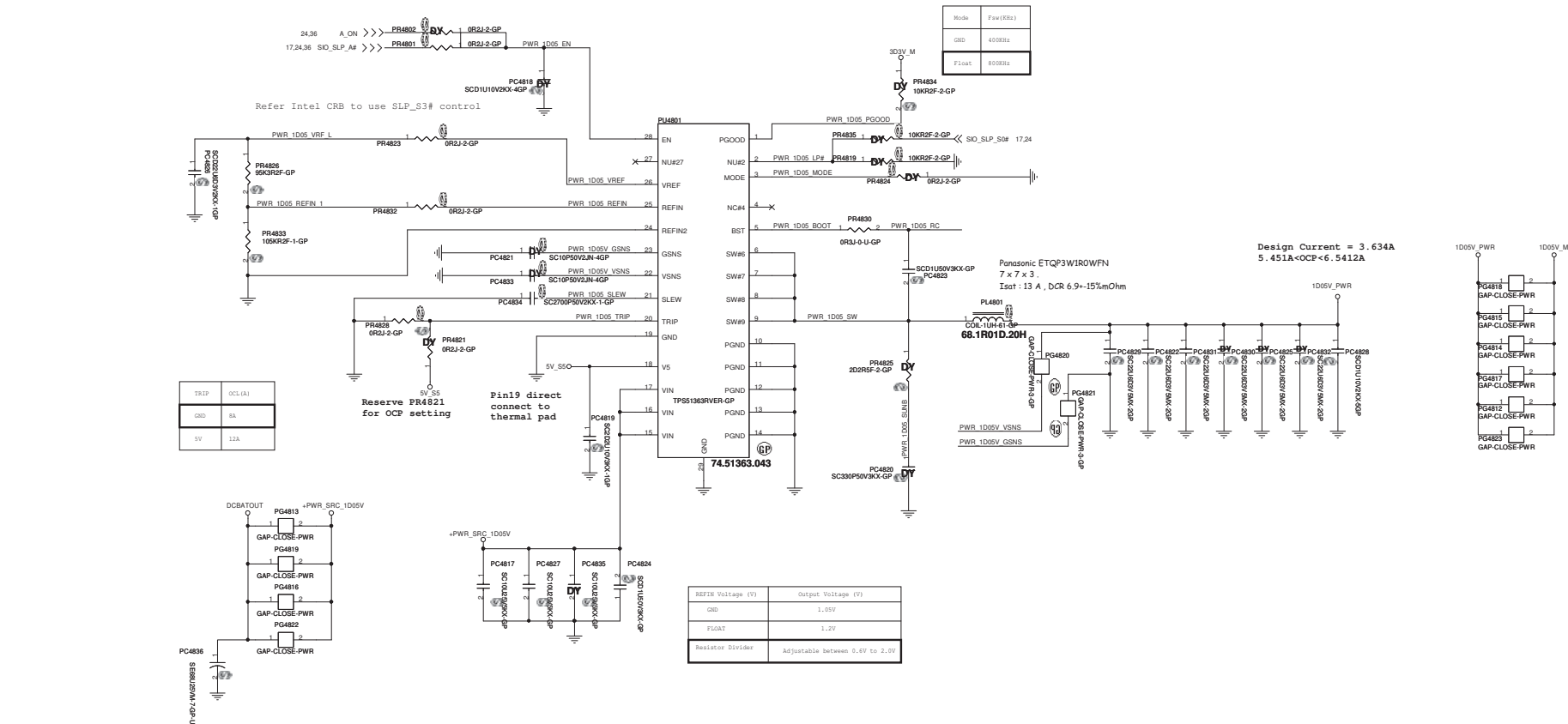
SSID = CPU.Regulator



For acoustic noise




<Core Design>




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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number		Rev
Round Rock 13.3" UMA			
Date: Friday, June 28, 2013	Sheet 50	of	107

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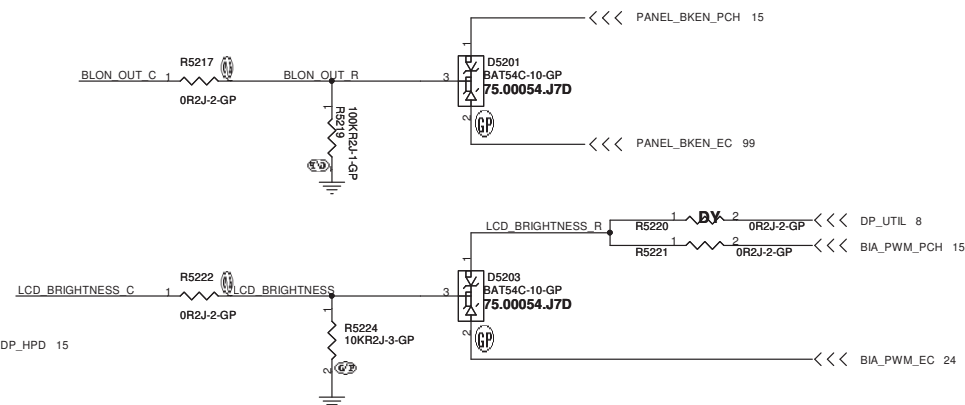
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number		Rev X00
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SSID = VIDEO



NOTE: EN has an internal pull down resistor to GND.



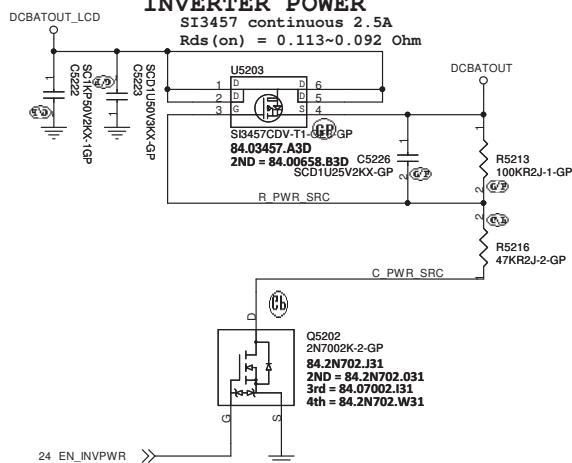
Camera Power



INVERTER POWER

SI3457 continuous 2.5A

Rds (on) = 0.113~0.092 Ohm



<Core Design>


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Title			
eDP Connector			
Size A3	Document Number	Rev	
Round Rock 13.3" U1A		000	
Date: Friday, June 28, 2013	Sheet 52	of	107

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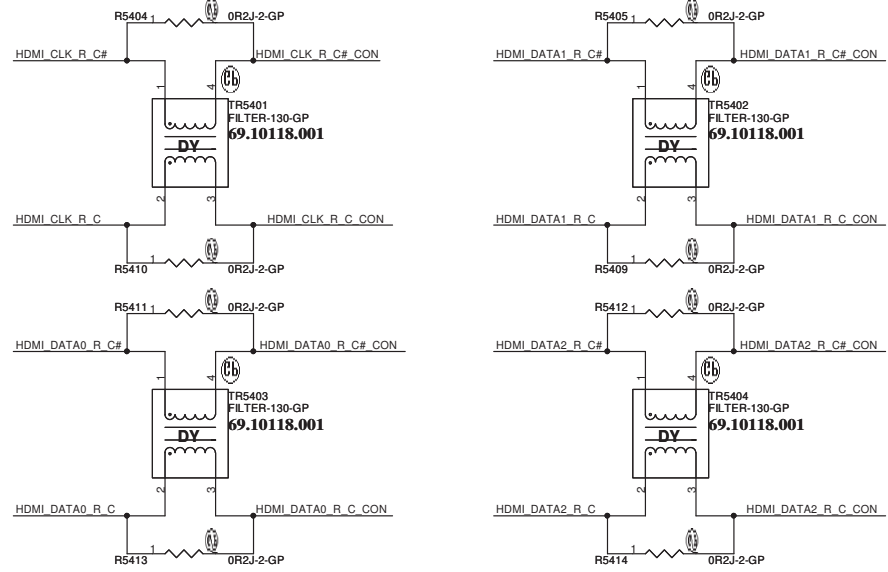
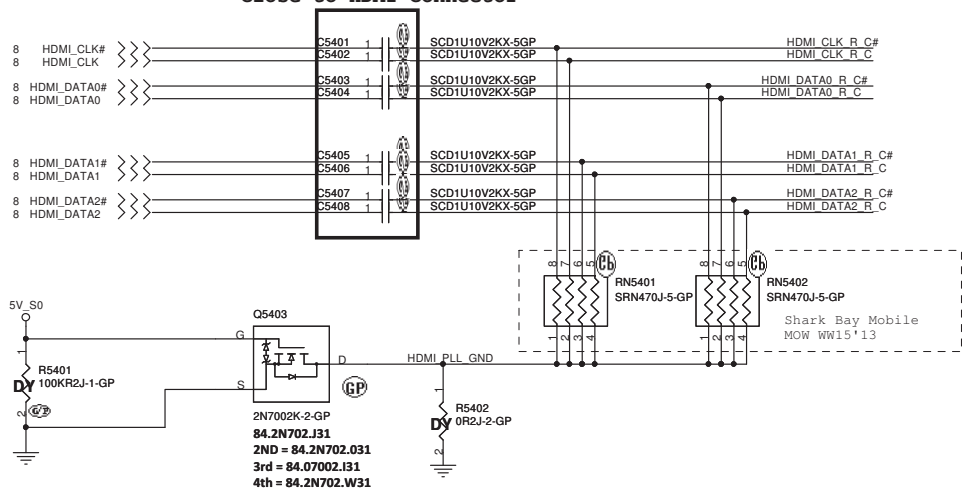
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number		Rev X00
Date: Friday, June 28, 2013		Sheet 53 of	107

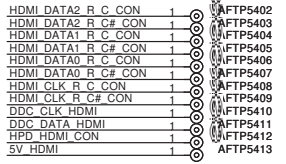
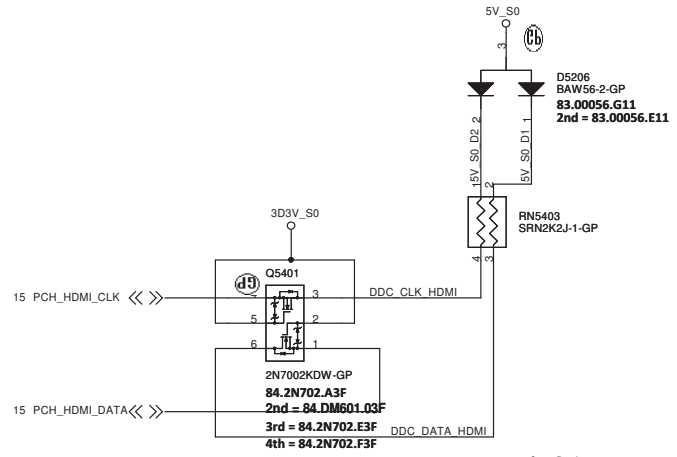
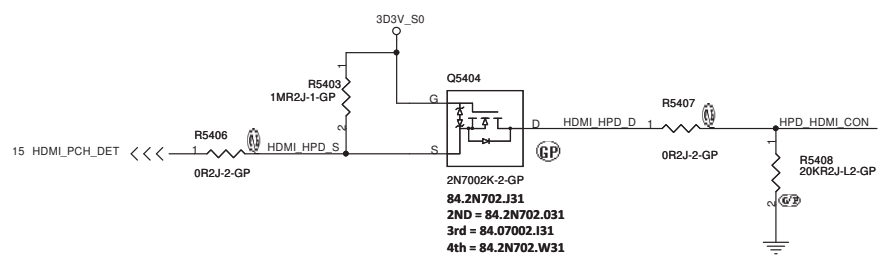
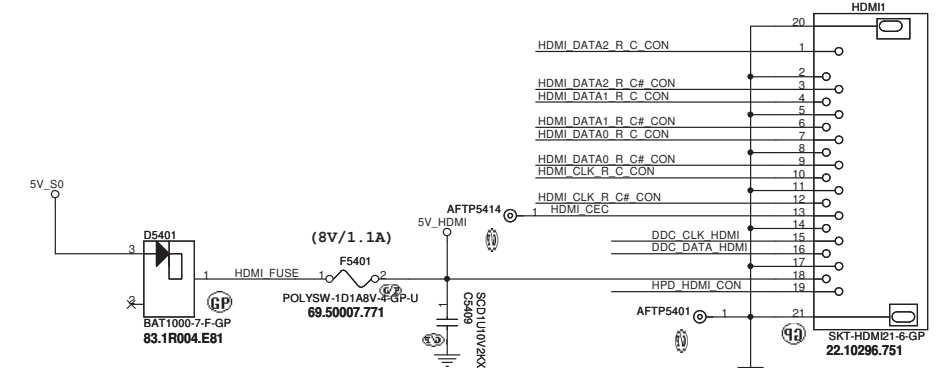
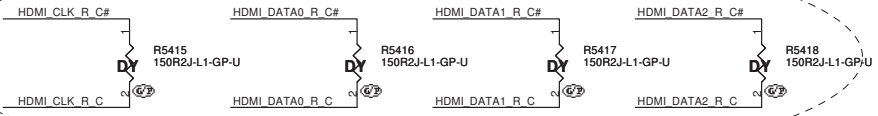
SSID = VIDEO

HDMI CONNECTOR

Close to HDMI Connector



SSI_0625



<Core Design>

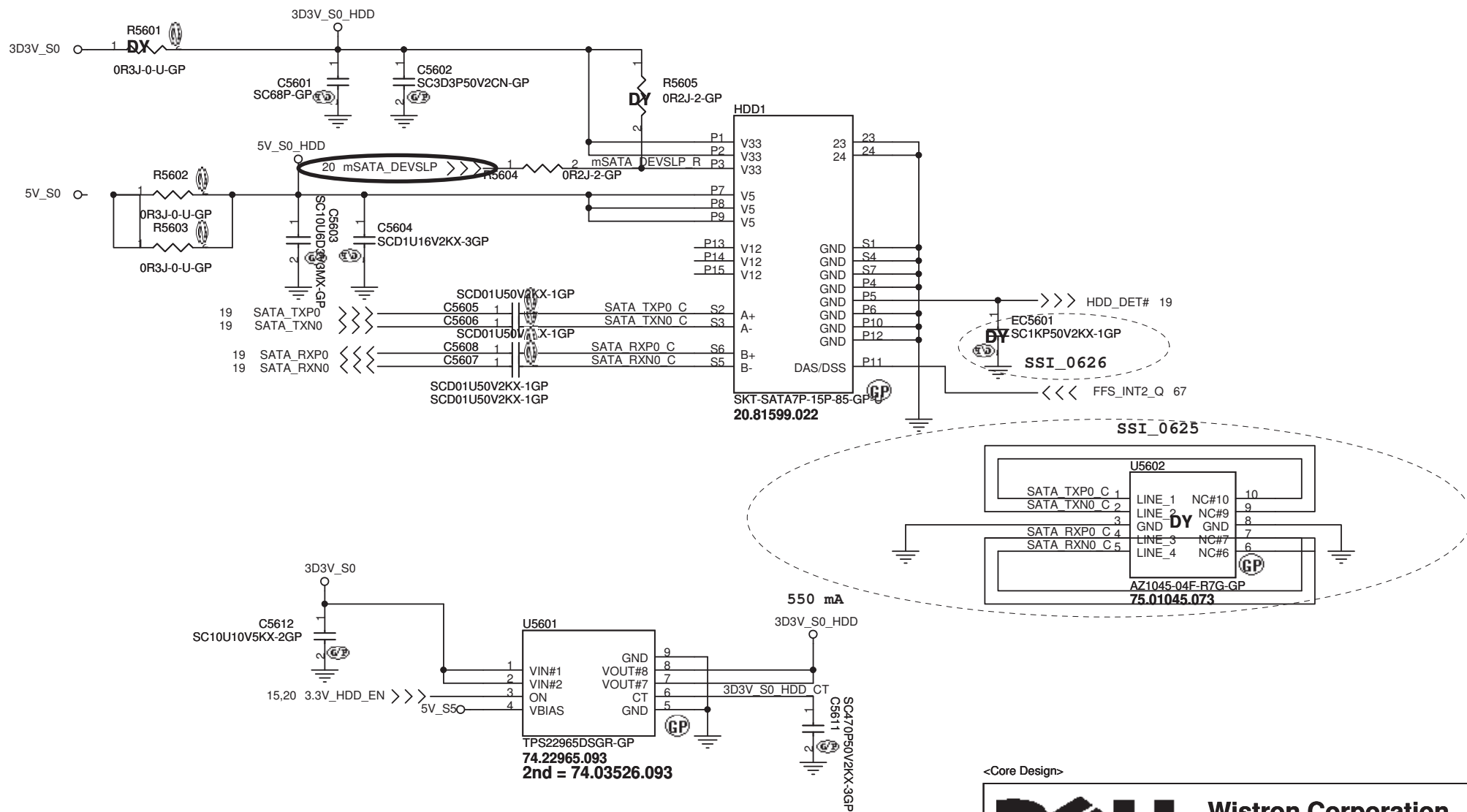
DELL Wistron Corporation
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Title **HDMI Level Shifter/Connector**

Size A3 Document Number **Round Rock 13.3" UMAX00**

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SSID = SATA



<Core Design>

DELL **Wistron Corporation**
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Title: **HDD**

Size: A4 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

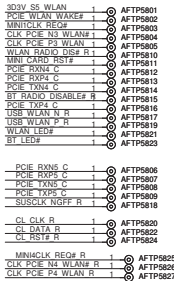
Date: Friday, June 28, 2013 Sheet 56 of 107

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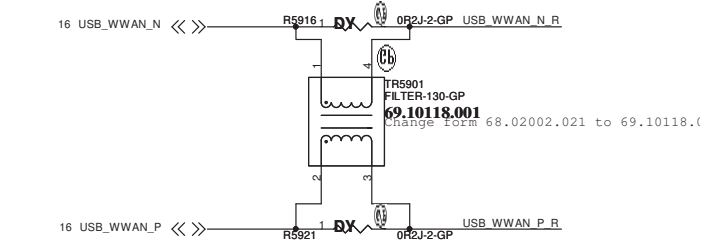
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Title			
Reserved			
Size A4	Document Number		Rev X00
Date: Friday, June 28, 2013		Sheet 57 of	107

SSID = WIRELESS



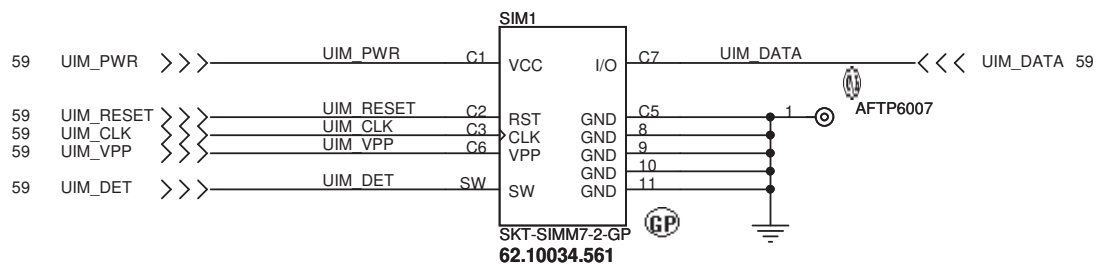
SC3 3P50V 2.1N 3GP
EC9811
#N7M SN POE KT0
SC3 3P50V 2.1N 3GP
EC9812
CLK POE P3 WLAN

SSID = WIRELESS

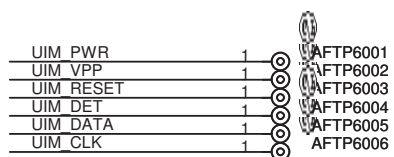


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Title			
NGFF-WWAN/SSD			
Size	Document Number		Rev
	Round Rock 13.3" UMA		X00
Date:	Friday, June 28, 2013	Sheet	59 of 107

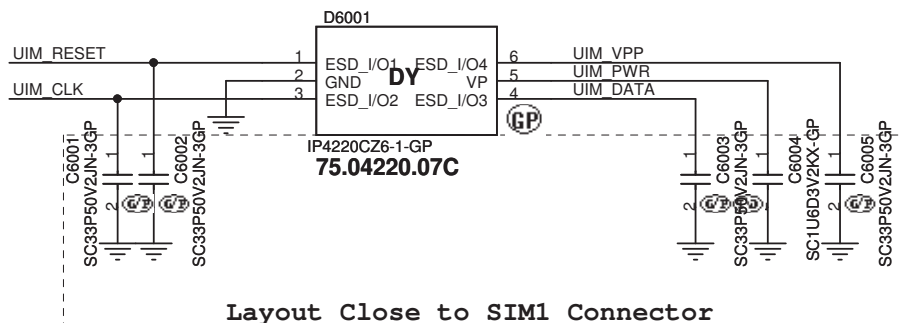
SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



Change from 83.00005.BAE to 75.04220.07C



Layout Close to SIM1 Connector

<Core Design>



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Title

mSATA

Size

Document Number

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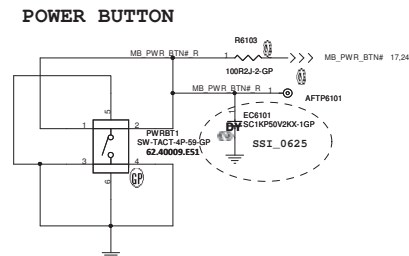
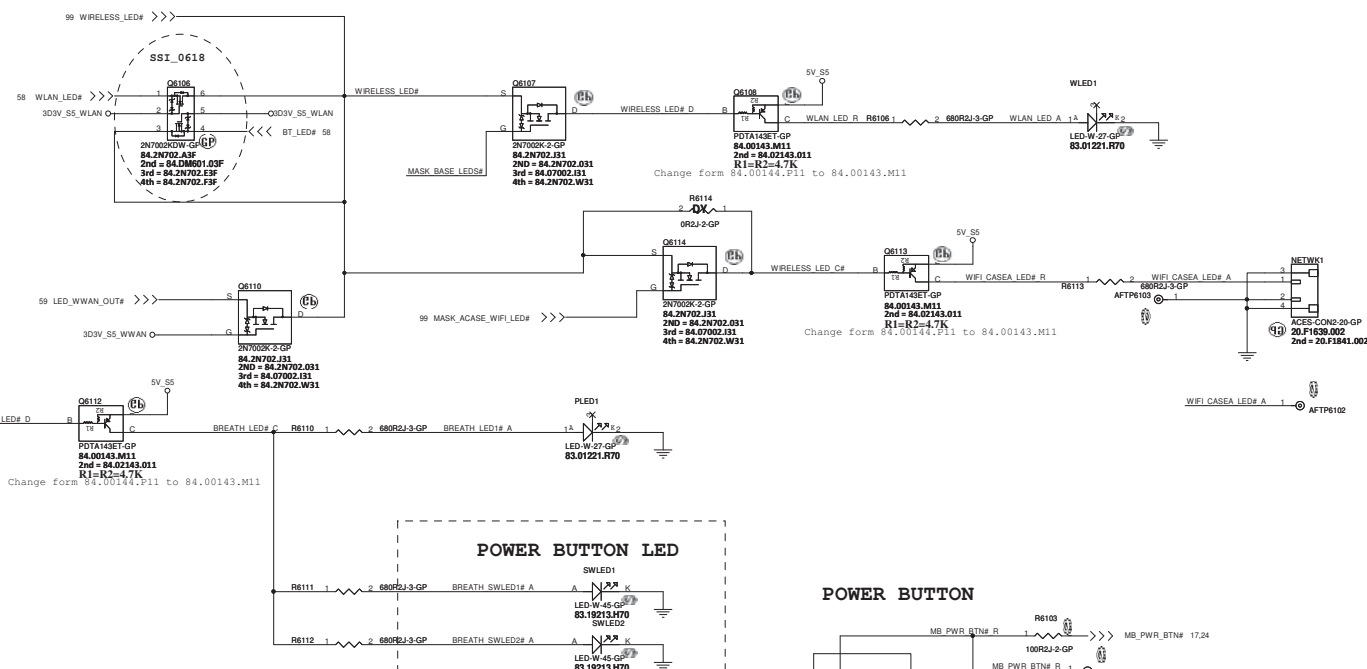
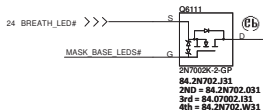
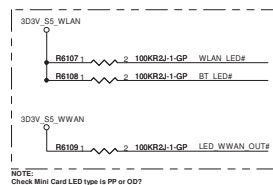
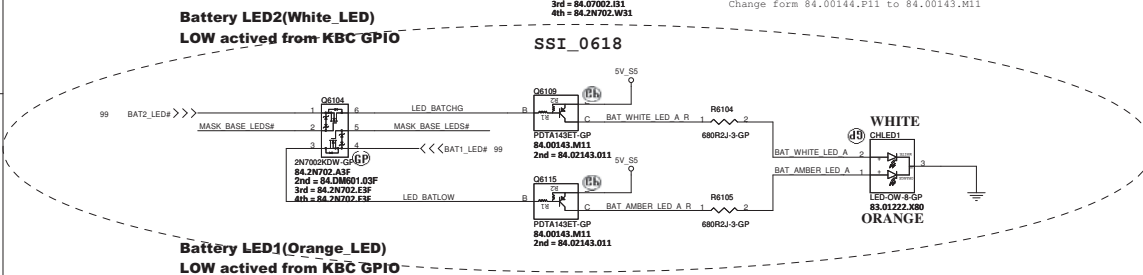
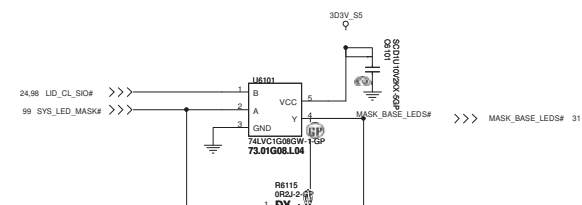
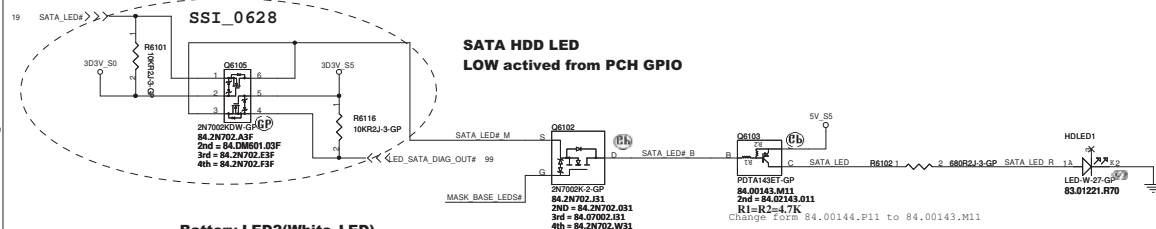
Rev

X00

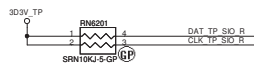
Date: Friday, June 28, 2013

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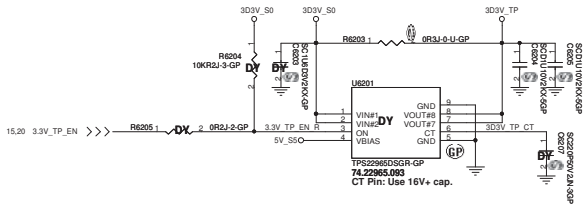
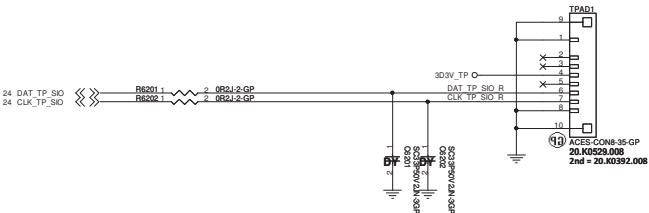
```
SSID = User.Interface
```



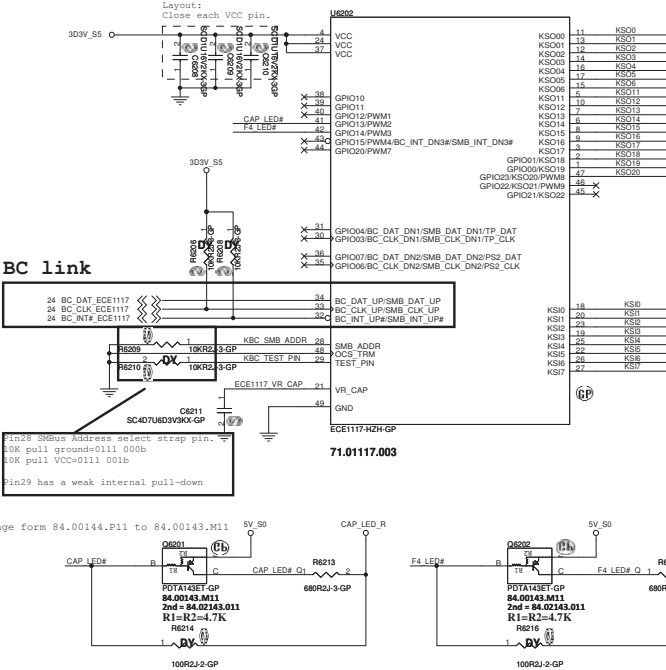
SSID = KBC SSID = Touch.Pad



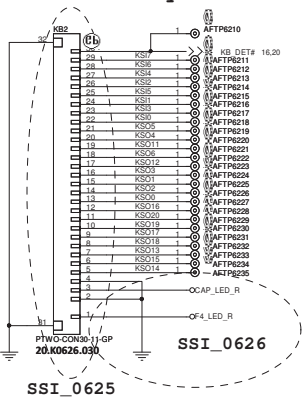
TouchPad Connector



KBC SMSC ECE1117




Internal KeyBoard Connector



MB Pin NO.	Description	Module Pin NO.
30	Diagnostic	1
29	KSI[7]:S8	2
28	KSI[6]:S7	3
27	KSI[4]:S5	4
26	KSI[2]:S3	5
25	KSI[5]:S6	6
24	KSI[1]:S2	7
23	KSI[3]:S4	8
22	KSI[0]:S1	9
21	KSO[5]:D6	10
20	KSO[4]:D5	11
19	KSO[11]:D8	12
18	KSO[6]:D7	13
17	KSO[12]:D9	14
16	KSO[3]:D4	15
15	KSO[1]:D2	16
14	KSO[2]:D3	17
13	KSO[0]:D1	18
12	KSO[16]:D13	19
11	KSO[20]:D17	20
10	KSO[19]:D16	21
9	KSO[17]:D14	22
8	KSO[18]:D15	23
7	KSO[13]:D10	24
6	KSO[15]:D12	25
5	KSO[14]:D11	26
4	GND	27
3	Caps Lock LED	28
2	GND	29
1	F4 LED	30


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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IO CONN			
Size A4	Document Number		Rev X00
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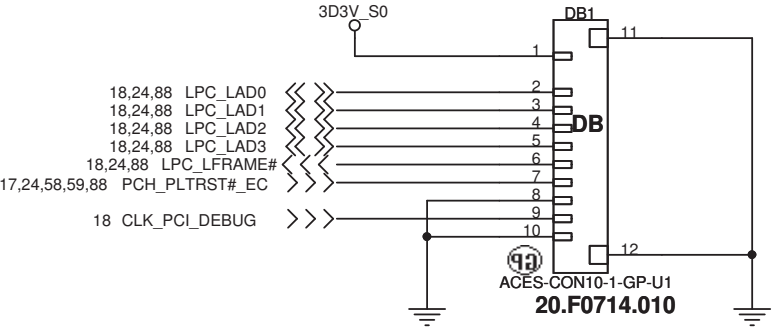
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<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Hall Sensor			
Size	Document Number		Rev
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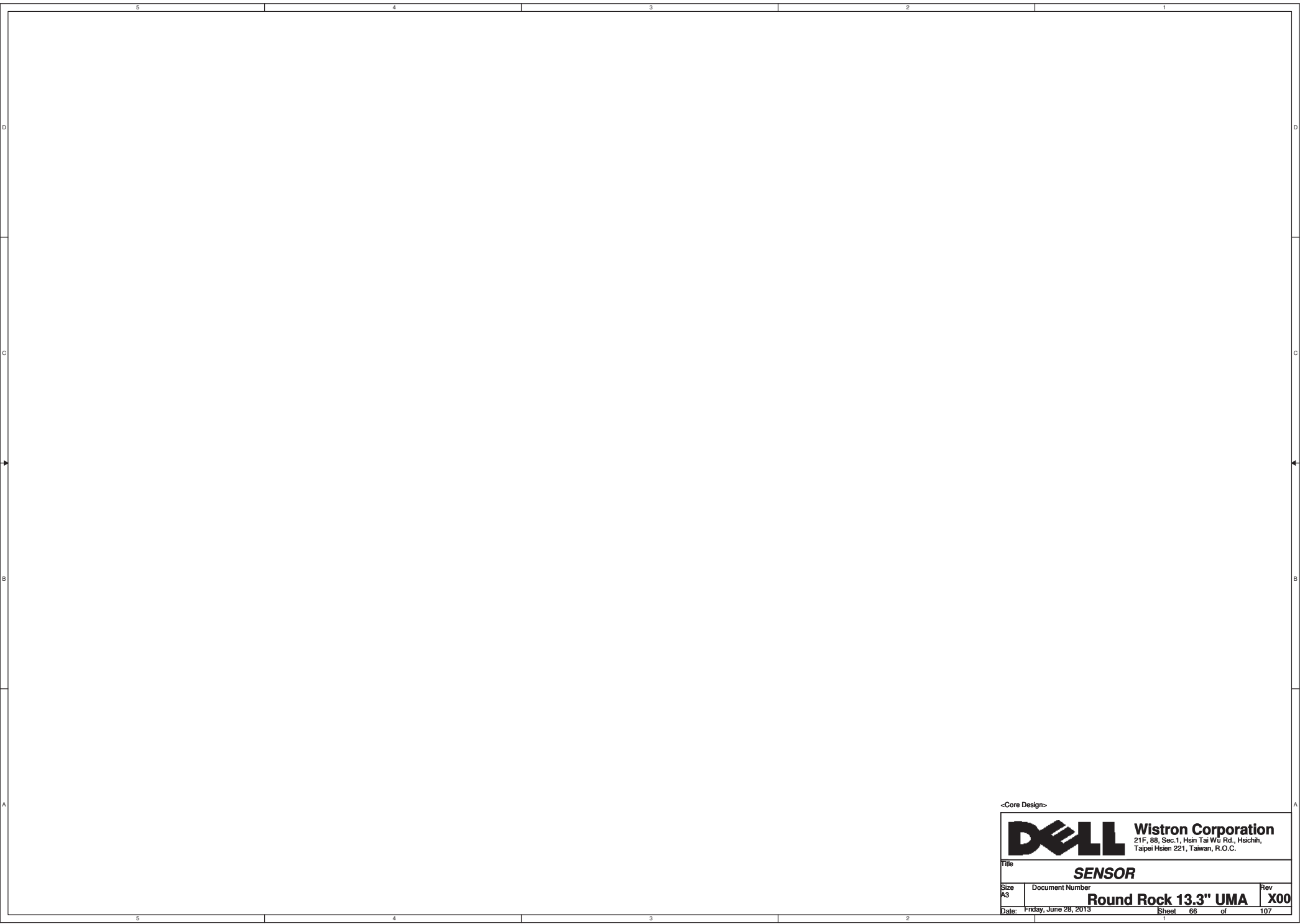
SSID = DEBUG PORT

SB modify to test pad




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Debug connector			
Size	Document Number		Rev
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<Core Design>



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Title

SENSOR

Size
A3

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<Core Design>



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Title

Thunderbolt (1/5)

Size	Document Number	Rev
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D					
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A					
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Thunderbolt (2/5)</i>			
Size A	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
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<Core Design>



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Title

Thunderbolt (3/5)

Size
A

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (4/5)

Size
A

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<Core Design>



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Title

Thunderbolt (5/5)

Size
A

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<Core Design>



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Title

GPU (1/5) PEG

Size
A

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C					
B					
A					
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<Core Design>



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Title

GPU (2/5) DIGITAL

Size A	Document Number Round Rock 13.3" UMA	Rev X00
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<Core Design>



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Title

GPU (3/5) VRAM

Size
A

Document Number

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D					
C					
B					
A					
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Title			
<i>GPU (4/5) GPIO</i>			
Size A	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
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<Core Design>



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Title

GPU (5/5) PWR/GND

Size
A

Document Number

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<Core Design>



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Title

VRAM1,2 (1/4)

Size
A

Document Number

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<Core Design>



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Title

VRAM3,4 (2/4)

Size
A

Document Number

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<Core Design>



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Title

VRAM5,6 (3/4)

Size
A

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<Core Design>



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Title

VRAM7,8 (4/4)

Size
A

Document Number

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D					
C					
B					
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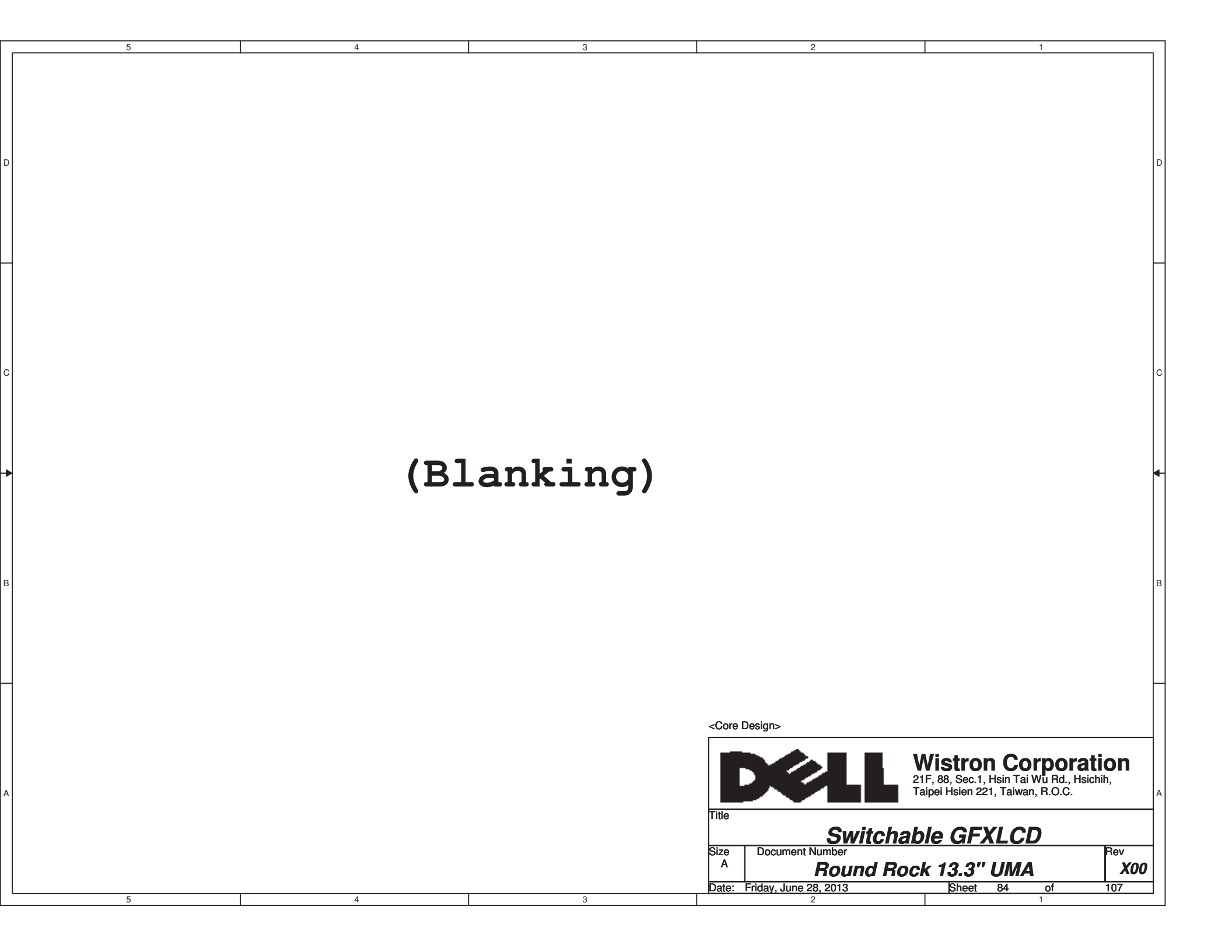
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Title VGA CORE		
Size A	Document Number Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013		Sheet 82 of 107

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D					
C					
B					
A					
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>DISCRETE VGAPOWER</i>			
Size A	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Switchable GFXLCD</i>			
Size A	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Switchable GFXCRT

Size
A

Document Number

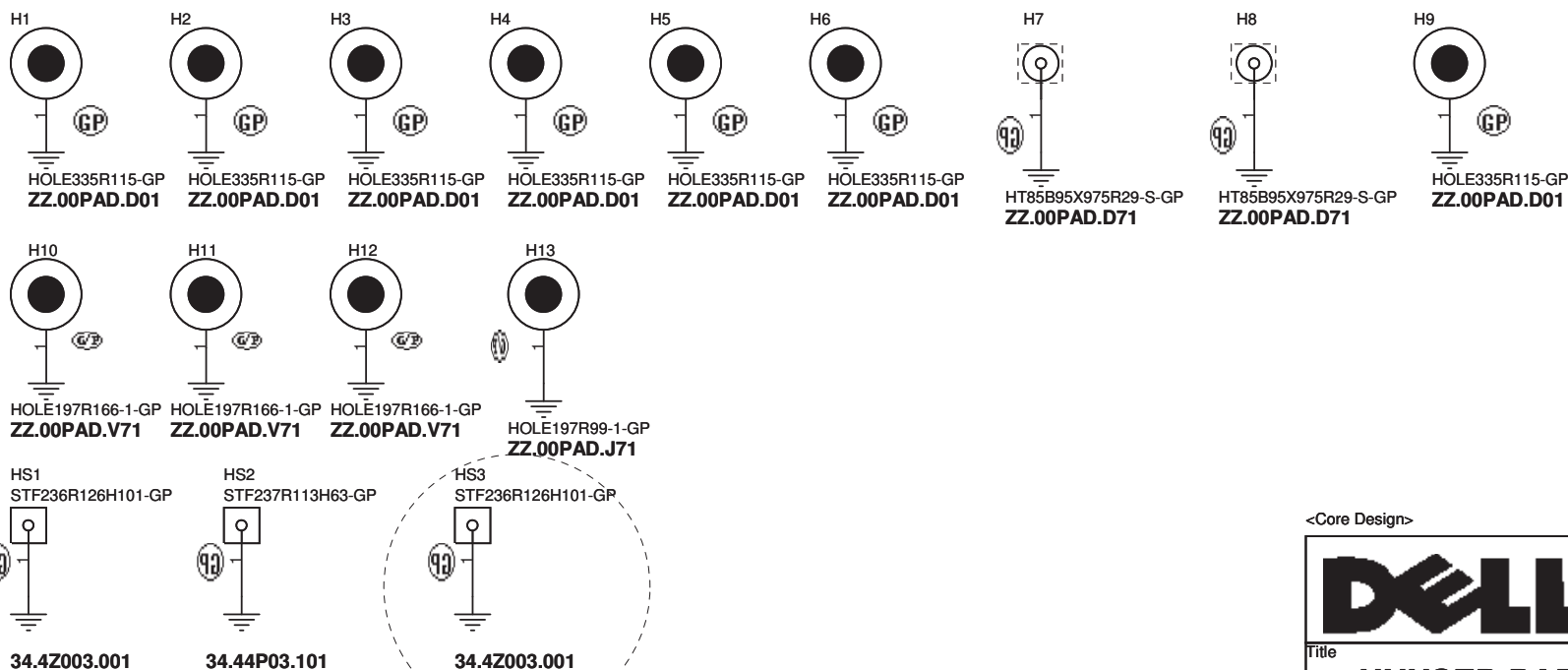
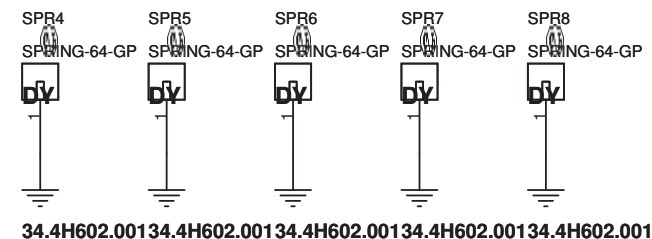
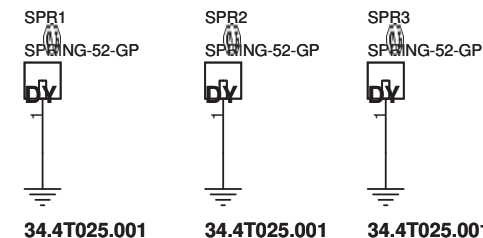
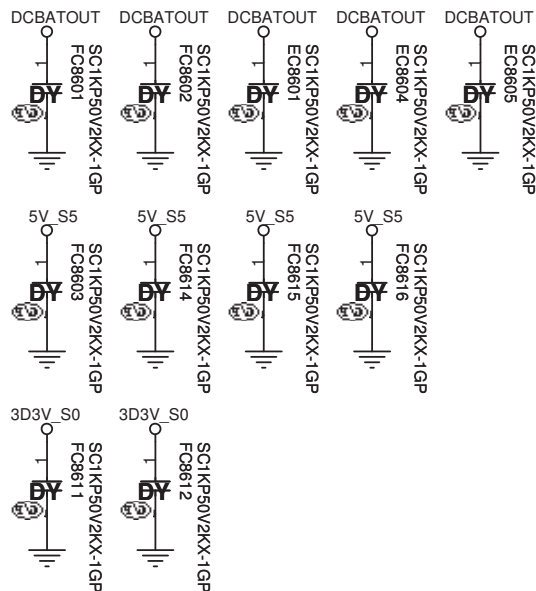
Round Rock 13.3" UMA

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<Core Design>



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Title

UNUSED PARTS/EMI Capacitors

Size

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SSID = USH

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<Core Design>



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Title

USH Board Connector

Size
A4

Document Number

Round Rock 13.3" UMA

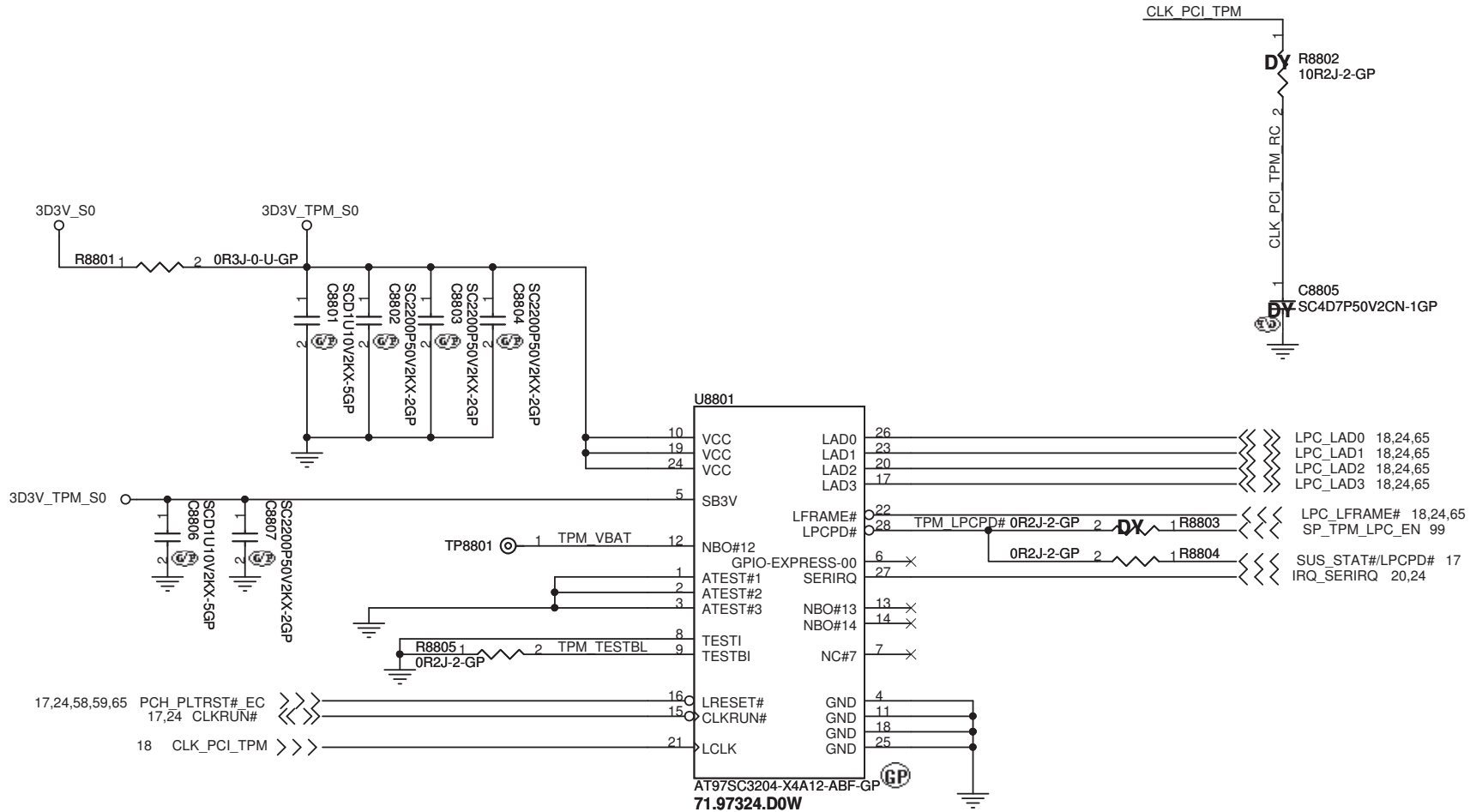
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Rev
X00

SSID = TPM

Place close to Pin 21



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Title

TPM

Size

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>NFC Connector</i>			
Size A4	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
Date: Friday, June 28, 2013		Sheet 90 of	107

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Smart Card			
Size	Document Number Round Rock 13.3" UMA		Rev X00
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	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

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Title			
<i>Reserved</i>			
Size A	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
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SSID = Docking

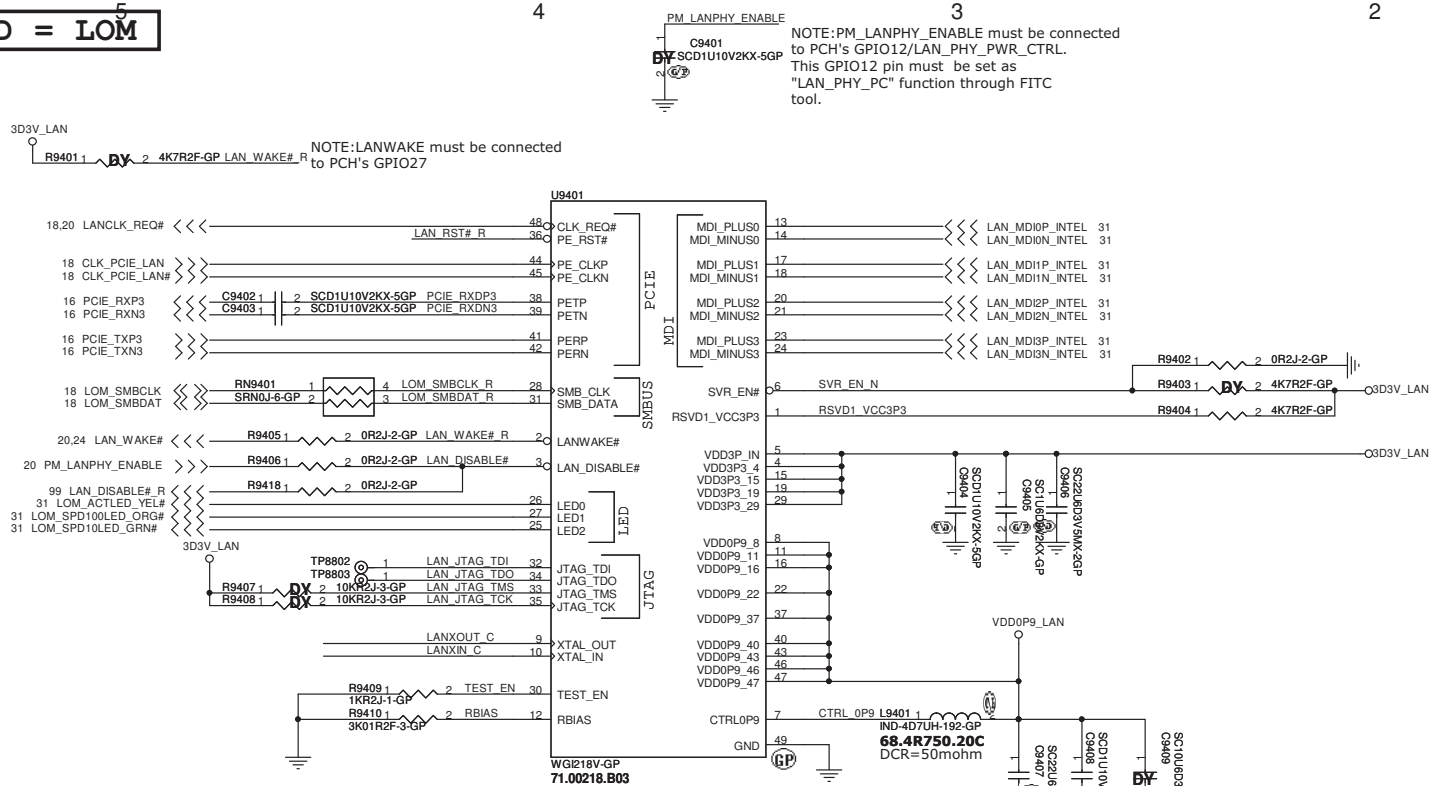
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<Core Design>

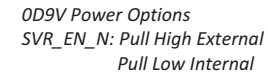


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Title			DOCKING	
Size	Document Number		Rev	
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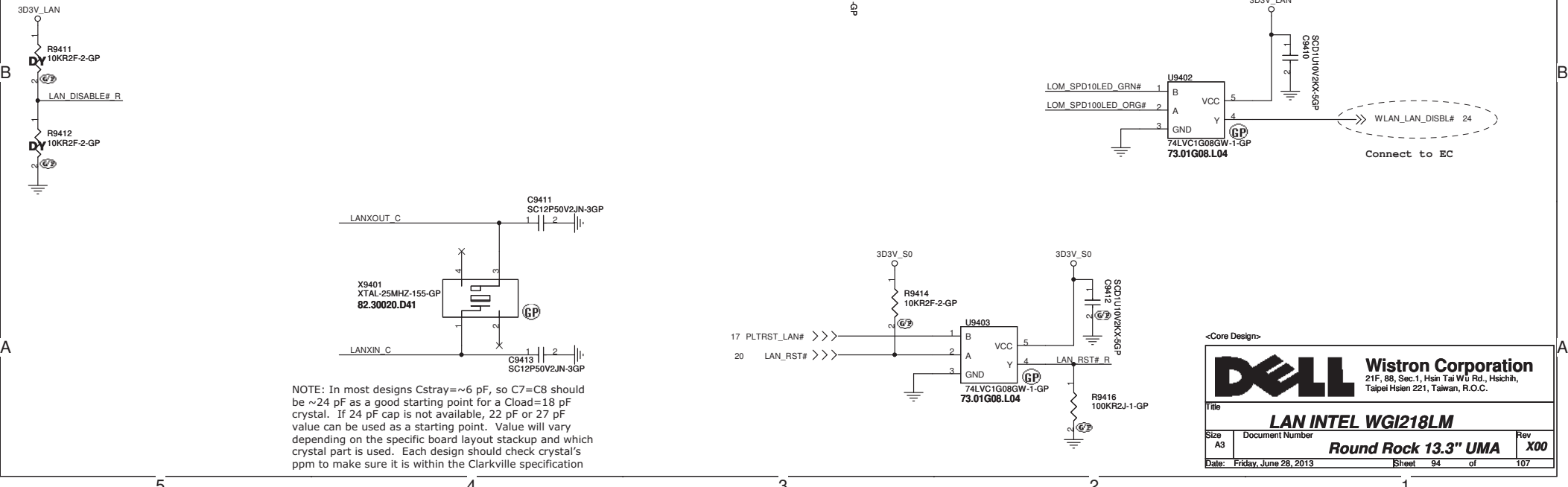
$$\text{SSID} = \text{LOM}^5$$


Note : LAN Chip must be changed to I218LM (71.00218.E03)




Internal SVR	Shared with external 1.05V SVR
L9401: STUFF	L9401: NO STUFF
R9413: NO STUFF	R9413: STUFF
R9402: STUFF	R9402: NO STUFF
R9403: NO STUFF	R9403: STUFF

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply. When sharing, make sure the 1.05V_LAN is controlled by the SLP_LAN signal.



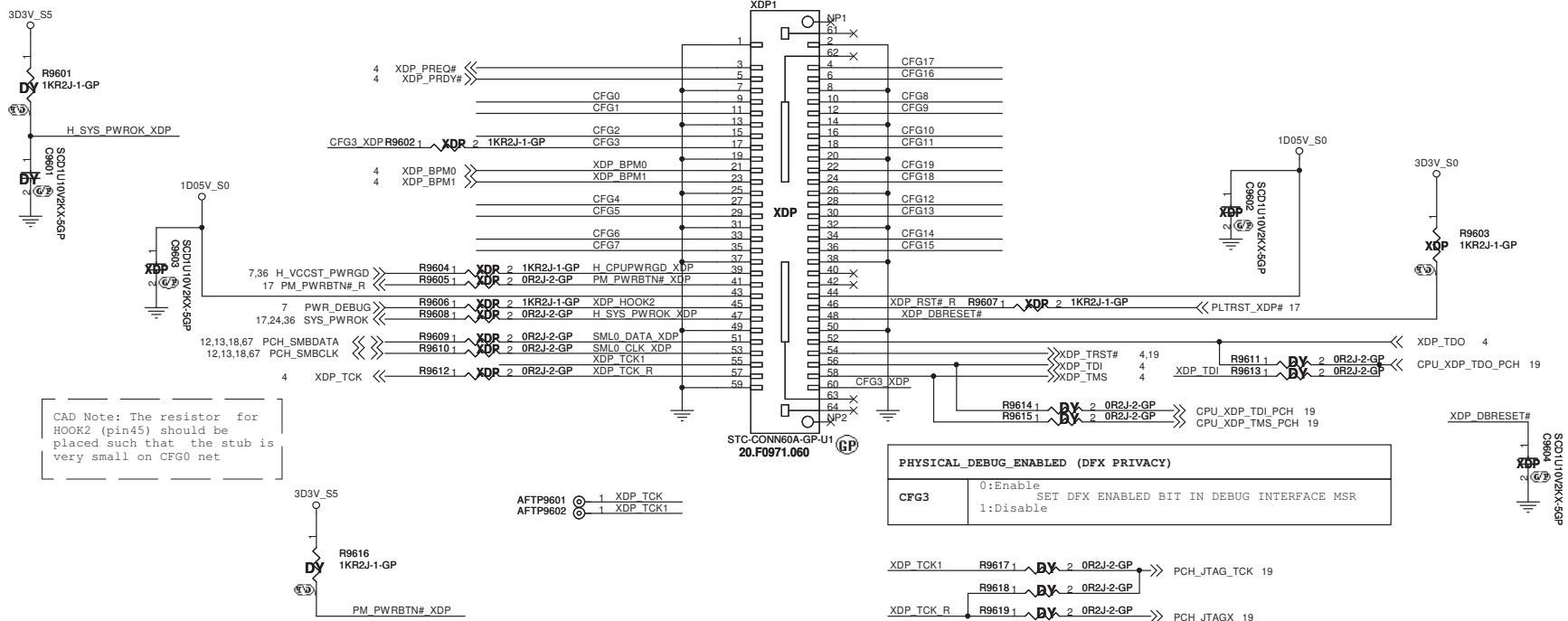
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Title			
LAN SW			
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SSID = CPU_XDP

CPU_XDP



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Title		CPU_XDP	
Size	Document Number	Rev	
A3		Round Rock 13.3" UMA	
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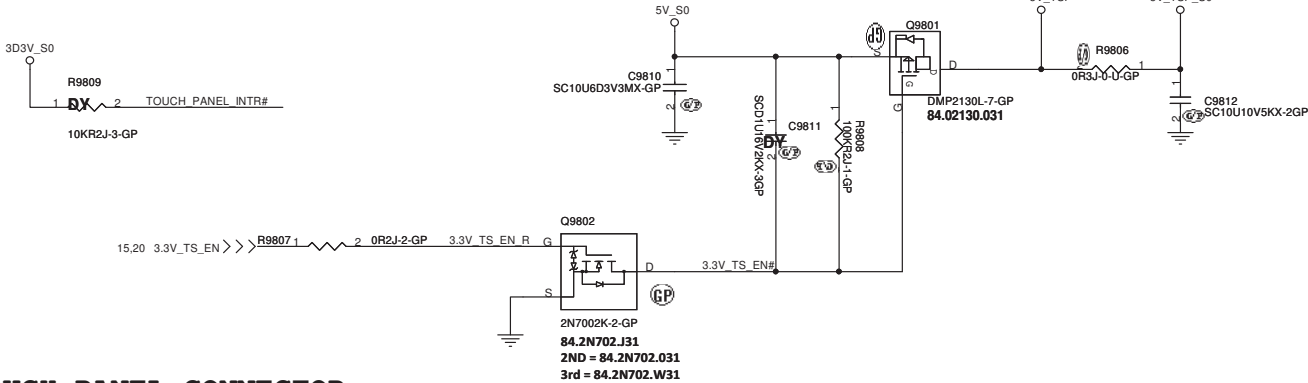
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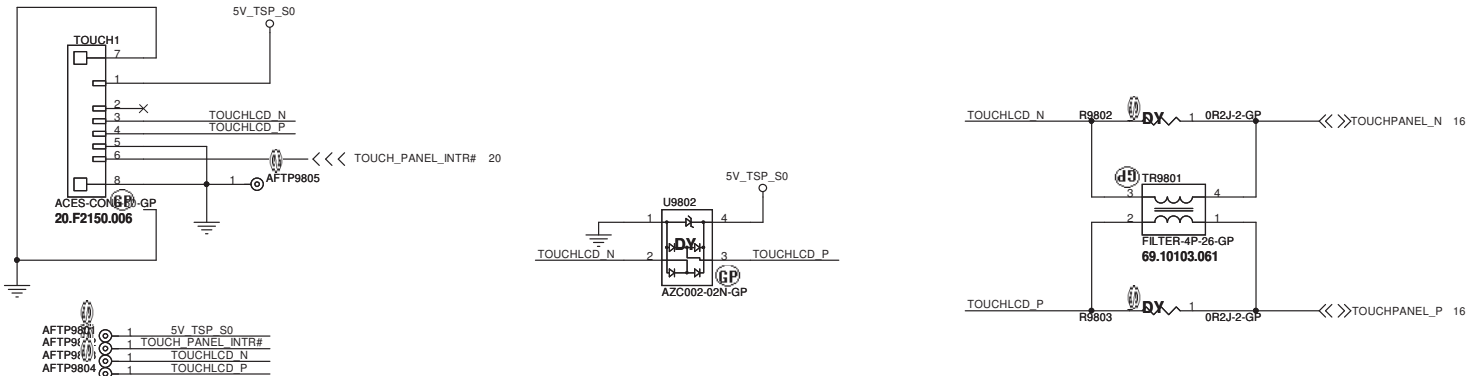
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB2.0 HUB			
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```
SSID = User.Interface
```

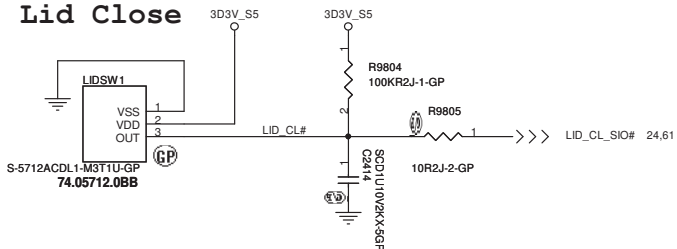
TOUCH PANEL POWER



TOUCH PANEL CONNECTOR



Lid Close



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Title	Author	Year	Journal	Volume	Page
...

Function Button

Size	Document Number
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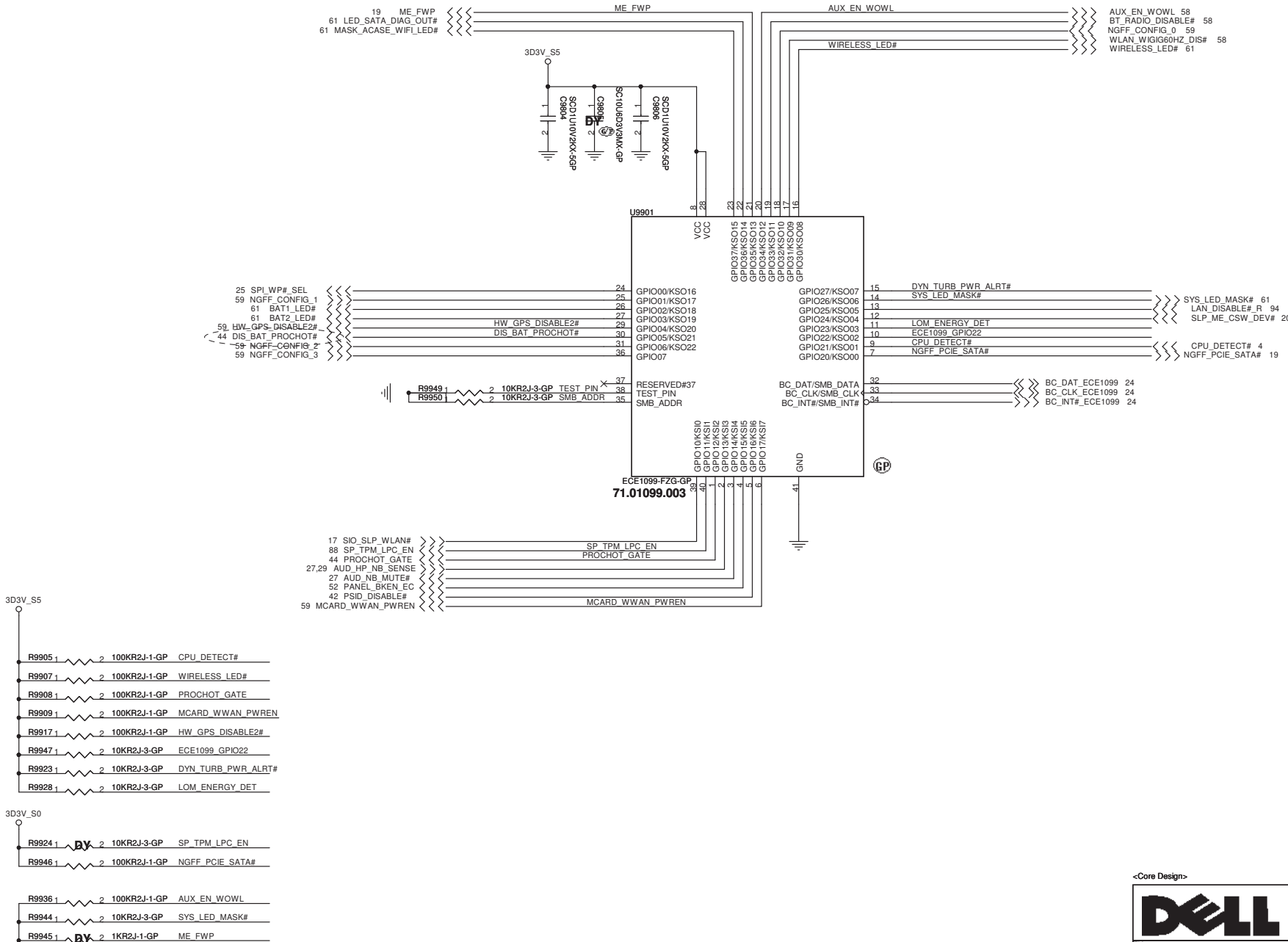
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Rev
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SSID = SIO



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Title

SIO - ECE1099Size
A3

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